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Characterization of p-CdTe/n-CdS hetero-junctions

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ABSTRACT

Nano-crystalline CdTe/CdS thin film hetero-junctions have been grown on glass substrate by thermal evaporation technique. The growth conditions to get stoichiometric compound films have been optimized. The grown hetero-junctions have been characterized for their *I–V* characteristics. Analysis of *I–V* characteristics has been made to investigate the current conduction mechanism in p-CdTe/n-CdS hetero-junction. The band gap energy of cadmium telluride and cadmium sulfide films have been computed from the study of variation of resistance with temperature. Based on the study, band diagram for p-CdTe/n-CdS hetero-junction has been proposed.

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1. Introduction

CdTe/CdS hetero-junction is most promising structure for photovoltaic applications. As deposited CdS is n-type and has wide band gap (~2.4 eV) making it suitable as a window layer [1]. CdTe has a band gap of ~1.5 eV, almost an ideal match for the solar spectrum making it well suited for use as the absorber layer. A good number of reports and reviews are available on the characterization of both CdTe films and CdTe/CdS devices [2–11]. Even though conversion efficiencies of more than 16% for small area laboratory cells have been achieved [10], as the efficiencies of industrial modules with large areas are still less than 10%, improving the fabrication technology is essential. The CdS/CdTe interface is believed to be a limiting factor for solar cell performance and the growth of a discrete region of intermediate composition has been used to explain limited cell efficiency [1]. Hence the detailed study of CdTe/CdS hetero-structure is essential to improve the cell performance. In present paper, characteristics like conduction mechanism of CdTe/CdS hetero-junction grown by thermal evaporation technique are reported.

2. Experimental

Both CdTe and CdS layers were deposited by thermal evaporation of stoichiometric powder of the compounds (99.99% pure from Aldrich Chem. Co.) in a residual pressure of 10^{-5} Torr. Thermally evaporated silver was used as the contact electrode. The *I–V* characteristics were recorded using computer interfaced Keithley 2400 source meter setup. Capacitance–frequency characteristics were recorded using Keithley 3322 LCZ meter. The variation of resistance with temperature was recorded using Keithley 2002 multimeter. All the measurements were done under dark condition and in air ambient.

3. Results and discussion

From trace of X-ray diffractogram, it was concluded that both CdTe and CdS films have cubic structure with preferred ⟨111⟩ orientation. Energy dispersive analysis of X-rays confirmed the stoichiometry of the films. Silver has been confirmed for the formation of ohmic contact with both CdTe and CdS. The typical *I–V* characteristic of

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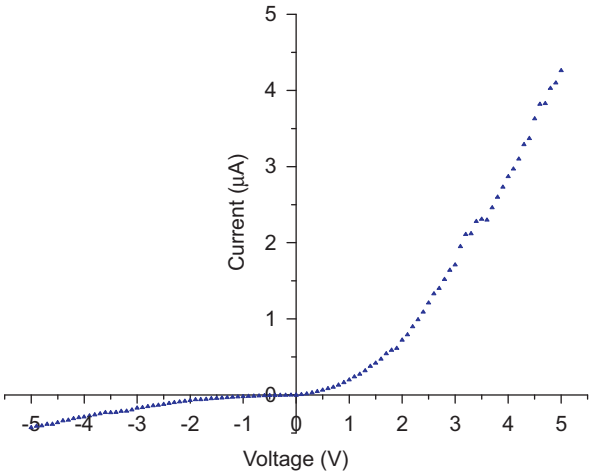

Fig. 1. *I–V* characteristics of p-CdTe/n-CdS hetero-junctions.

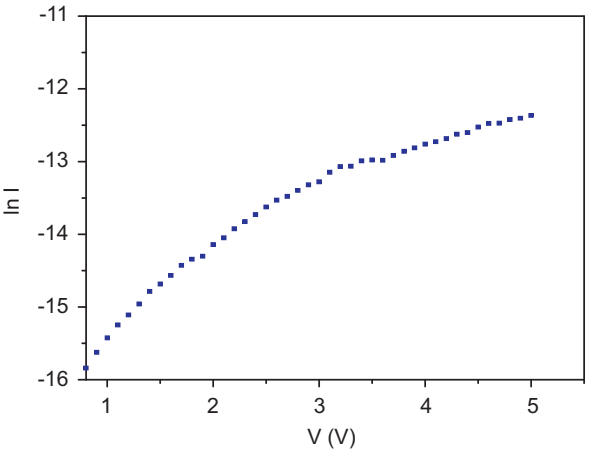

Fig. 3. ln*I* vs. *V* at higher voltages for p-CdTe/n-CdS hetero-junctions.

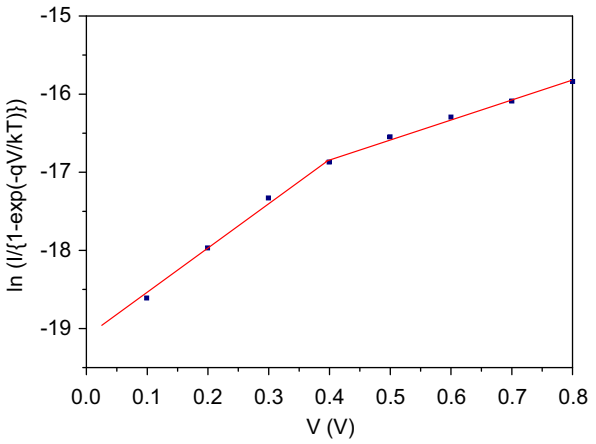

Fig. 2. $\ln[I/\{1-\exp(-qV/kT)\}]$ vs. *V* at lower voltages for p-CdTe/n-CdS hetero-junctions.

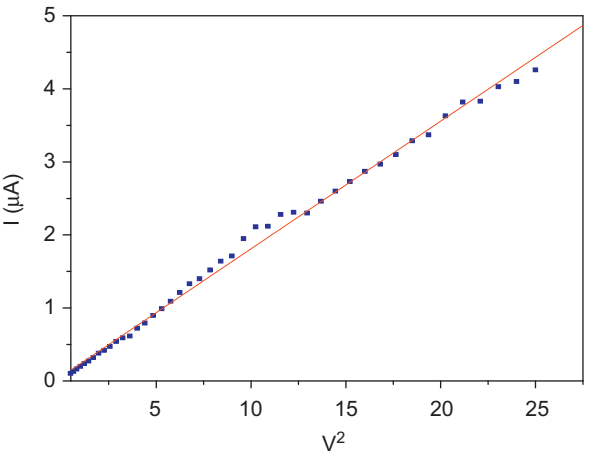

Fig. 4. *I* vs. V^2 for p-CdTe/n-CdS hetero-junctions at higher voltages.

p-CdTe/n-CdS hetero-junction is shown in Fig. 1. A detailed analysis of *I–V* characteristics has been made to establish the current flow mechanism.

Under certain circumstances it may be possible for charge carriers with energies below the top of the barrier to penetrate the barrier by quantum-mechanical tunneling. In case of tunneling dominated conduction, current is described by the following relation [5]:

$$I = I_0 \exp(BT) \exp(AV) \tag{1}$$

where I_0, A and B are constants, V is the applied bias voltage and T is the temperature in absolute scale. Tunneling dominates the current flow mechanism only in the case of high carrier concentration (about 10^{18}–$10^{19}\,cm^{-3}$) [5]. But in the present case, the carrier concentration is much lower than this as observed by hall measurement (10^{14}–$10^{15}\,cm^{-3}$). Hence, tunneling may not be the dominating mechanism.

Recombination at interface is the another possible way of conduction where current can be described by the following relation [12]:

$$I = I_S \exp\left(\frac{qV}{nkT}\right)\left\{1 - \exp\left(\frac{-qV}{kT}\right)\right\} \tag{2}$$

where I_S is the reverse saturation current, k is Boltzmann constant, q is the electronic charge and n is the ideality factor. Plot of $\ln I/\{1-\exp(-qV/kT)\}$ vs. V at lower voltages is shown in Fig. 2. Fitting of the experimental data to the above equation indicates that current transport is dominated by recombination at the interface. Recombination is the process where an electron moves from the conduction band to the valence band so that a mobile electron–hole pair disappear. Normally volume impurities and surface imperfections are the sites of recombination. The recombination component of the current is likely to be more important in high barriers, in material of low life time, at low temperatures and at low forward voltages [12]. Fig. 2 shows two distinct regions of conduction, having different values of n. At lower voltages ($V<0.4\,V$), n is 1.38 whereas at higher voltages, it is 2.68. It has been reported that recombination of carriers at the interface due to the

defects produced by lattice mismatch and ohmic losses lead to higher ideality factor [13]. Mahammad Hussain and Jayarama Reddy [14] also have observed recombination dominated current transport mechanism at lower voltages in CdS/CdTe hetero-junctions. But they have reported higher value of ideality factor (about 4.62) for the junction. Higher ideality factor is the indication of the deviation of diode characteristics from the ideal diode characteristics. For higher voltages, Eq. (2) can be approximated as [15]

$$I = I_S \exp\left(\frac{qV}{nkT}\right) \tag{3}$$

The plot of $\ln I$ vs. V for the junction at higher voltages is shown in Fig. 3. Non-linearity in the plot at higher voltage region rules out the current conduction by recombination mechanism in this region.

At higher voltages, current varies as square of the voltage (Fig. 4). This suggests that, in this region, current is controlled by space charge limited conduction (SCLC) and allows us to use space charge limited (SCL) theory for I–V analysis [16]. In the SCLC region, current can be related to the voltage as follows [17]:

$$I = \frac{\varepsilon_r N_C}{8L^3 N_t} A\mu\varepsilon V^2 \exp(-E_t/kT) \tag{4}$$

where ε_r is the relative permittivity, N_C is the effective density of states, N_t is the concentration of traps with activation energy E_t, L is the film thickness, A is the device area, μ is the mobility and ε is the permittivity. This mode of conduction can have a pronounced effect on the electrical properties of semiconductors at room temperature and below, because they normally have a low density of free carriers and charge unbalance can be easily produced by an applied voltage. The character and magnitude of space-charge limited effects are determined largely by the presence of localized states which can trap and store charge in equilibrium with the free charge. Single carrier injected currents are necessarily space-charge limited and in a perfect trap-free insulator where all the injected carriers remain free and all contribute to the space-charge, the current flow is exactly analogous to that in a vacuum diode. The presence of traps generally

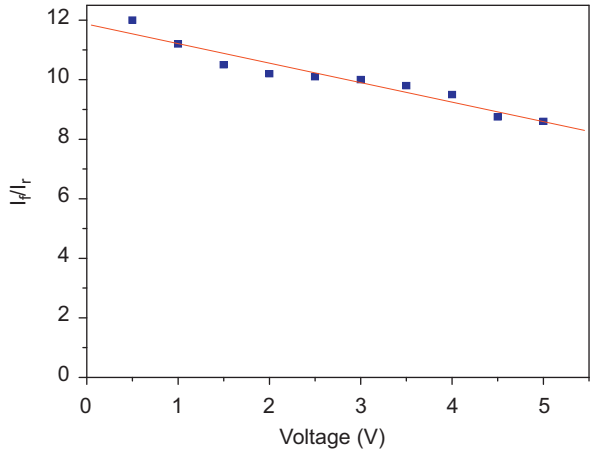

Fig. 5. Variation of rectification ratio with bias voltage for p-CdTe/n-CdS hetero-junctions.

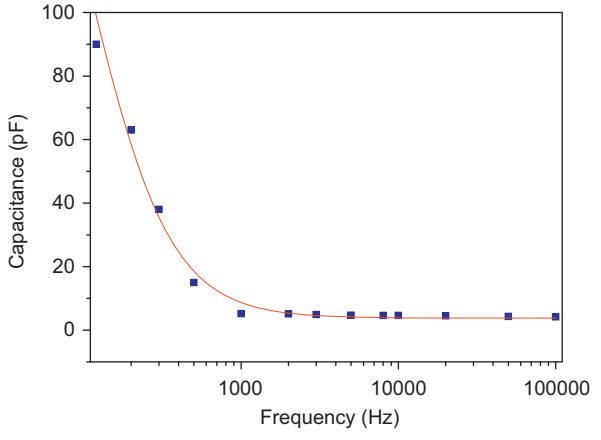

Fig. 6. Variation of junction capacitance with frequency for p-CdTe/n-CdS hetero-junctions.

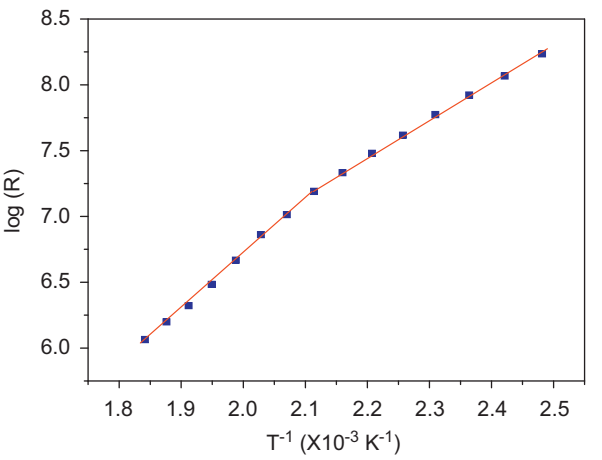

Fig. 7. Plot of $\log(R)$ vs. T^{-1} for CdTe films deposited at 300 K.

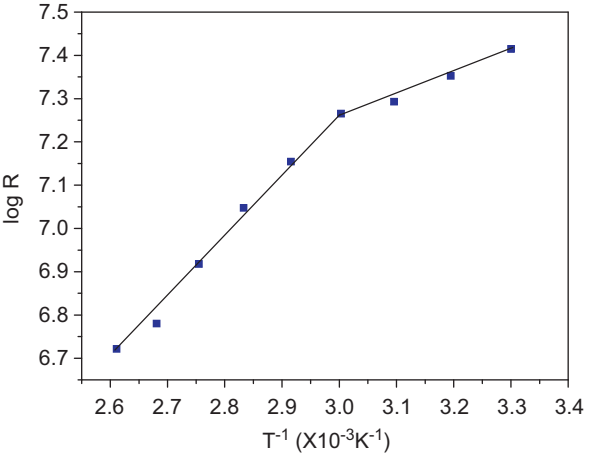

Fig. 8. Plot of $\log(R)$ vs. T^{-1} for CdS films deposited at 300 K.

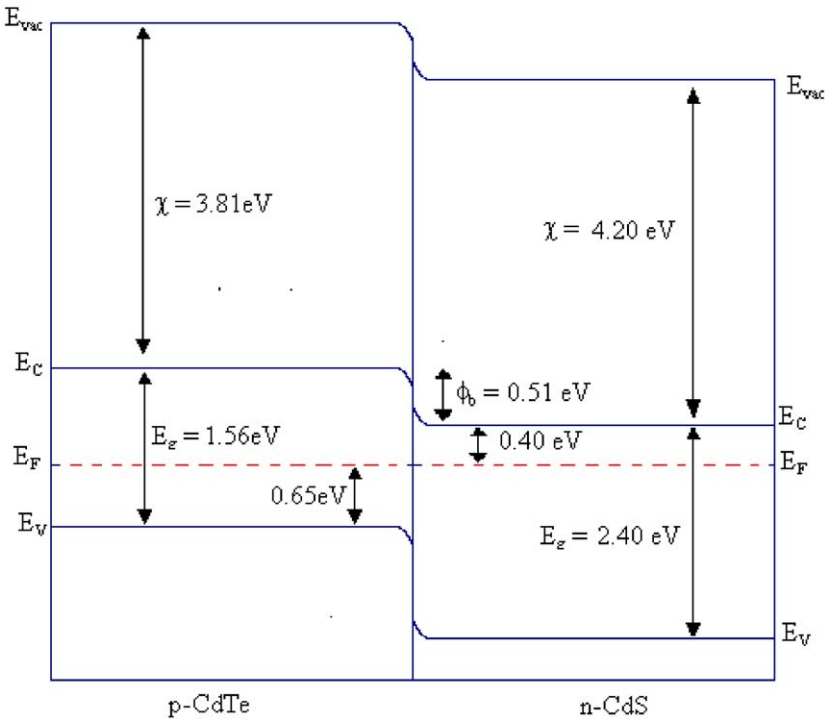

Fig. 9. Proposed band diagram of p-CdTe/n-CdS hetero-junction.

reduces the current by capturing most of the injected carriers. As the injection level (applied voltage) is raised all the traps will eventually become filled and the current will rise sharply back to the trap-free value.

Rectification ratio, the ratio of magnitude of forward current to reverse current, was observed to reduce slightly with increase in bias voltage (Fig. 5). The variation of junction capacitance with frequency is shown in Fig. 6, which shows the decrease in capacitance with frequency. Similar observation is reported for n-$Cd_{0.9}Zn_{0.1}S$/p-CdTe hetero-junctions [14]. As the measuring frequency is decreased more deep levels at or near the interface are able to respond to the ac signal, hence generating a larger capacitance.

Plot of $\log(R)$ vs. T^{-1} for CdTe and CdS films deposited at 300 K are shown in Figs. 7 and 8, respectively. The band gap energy computed from the study of variation of electrical resistivity with temperature yielded a value of 1.56 eV for CdTe films. The thermal activation energy of extrinsic region was found to be 0.65 eV. Band gap and thermal activation energy of extrinsic region for CdS films were 2.4 and 0.4 eV, respectively. Based on these data, band diagram for p-CdTe/n-CdS junction has been proposed (Fig. 9).

4. Conclusions

CdTe/CdS hetero-structure shows good rectification. Recombination at interface dominates the current conduction at lower voltages whereas space charge limited conduction controls the current conduction at higher voltages. It is observed that the rectification ratio reduces slightly with bias voltage implying the possible application at relatively lower voltages. The junction capacitance has shown higher value at lower frequencies due to deep levels at or near the interface and decreased with increase in frequency. Based on the study, band diagram for CdTe/CdS hetero-junction has been proposed.

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