Reconfigurable highly efficient CMOS-based dual input variable output switched capacitor converter for low power applications

C. Abraham✉, V. Subburaj, D. Jena, P. Perumal, B. R. Jose and J. Mathew

A reconfigurable switched capacitor converter (SCC) topology with nine/ten CMOS switches and two flying capacitors is presented. It is capable of accepting two input sources simultaneously with an input voltage in the range of 1–2.5 V and delivers the output for 15 conversion ratios. The proposed SCC can drive a load current ranging from 10 µA to 10 mA at an open loop efficiency of >90%. One of the important applications of the proposed converter is the utilisation of photovoltaic (PV) or the combination of PV and other direct current sources. The regulation of the output voltage can be achieved either by changing the voltage conversion ratios or using variable switching frequency.

Introduction: Fully integrated portable voltage regulators are gaining popularity in global power supplies, renewable energy conditioning, bio-medical applications and so on, due to their miniaturised form with regulation capabilities to operate using a single integrated circuit [1]. The proposed converter in this Letter is capable of delivering 15 output voltage conversion ratios (VCRs). By reconfiguring the switches and flying capacitor connections, different targeted output voltages are generated to operate with low input/output voltages. The proof of validation has been confirmed by mathematical, simulation and hardware prototype results.

Proposed CMOS-based switched capacitor converter (SCC) architecture: The layout of the proposed SCC is shown in Fig. 1*a*. It works for 13 VCRs using nine CMOS switches S_{b1}–S_{b9}, two flying capacitors (C_{fly1} and C_{fly2}) and one filter capacitor C_{out}. In addition, two more VCRs are discussed in later sections, but using ten switches. For each VCR, a predetermined pulse sequence is generated for controlling the switches as given in Table 1. Two phases (ϕ_c and ϕ_t), with 50% duty cycle, are used to charge and discharge the capacitors as shown in Fig. 1*a*. The work presented in [2] has 14 switches, which includes four diodes that can considerably lower the efficiency due to the forward diode voltage drop. Therefore the attempt in this Letter is to generate 15 against 11 VCRs in [2], using only nine/ten CMOS switches and no diodes. This reduces the component count which increases efficiency at the same time requiring less chip space.

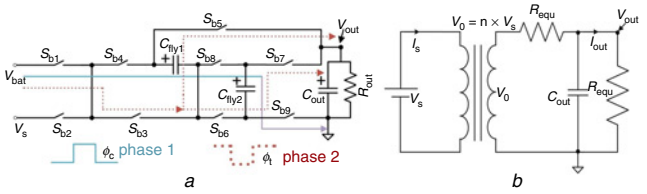

Fig. 1 *Proposed SCC circuit schematic and model*
a Proposed buck-boost SCC
b SCC equivalent circuit model [2, 3]

Table 1: 13 states and VCRs of proposed converter

States	VCRs	S_{b1}	S_{b2}	S_{b3}	S_{b4}	S_{b5}	S_{b6}	S_{b7}	S_{b8}	S_{b9}
1	$V_{bat} \times 2$	1	–	ϕ_t	ϕ_c	ϕ_t	ϕ_c	–	–	ϕ_c
2	$V_s \times 2$	–	1	ϕ_t	ϕ_c	ϕ_t	ϕ_c	–	–	ϕ_c
3	$V_s + V_{bat}$	ϕ_c	ϕ_t	ϕ_t	ϕ_c	ϕ_t	ϕ_c	–	–	ϕ_c
4	$V_{bat} \times 1.5$	–	1	ϕ_t	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	ϕ_c
5	$V_s \times 1.5$	1	–	ϕ_t	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	ϕ_c
6	$V_s + (0.5V_{bat})$	ϕ_c	ϕ_t	ϕ_t	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	ϕ_c
7	$V_{bat} + (0.5V_s)$	ϕ_t	ϕ_c	ϕ_t	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	ϕ_c
8	$V_{bat} \times 0.5$	ϕ_c	–	–	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	1
9	$V_s \times 0.5$	–	ϕ_c	–	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	1
10	V_{bat}	ϕ_c	–	–	ϕ_c	ϕ_t	1	–	–	1
11	V_s	–	ϕ_c	–	ϕ_c	ϕ_t	1	–	–	1
12	$(V_{bat} + V_s) \times 0.5$	ϕ_c	ϕ_t	ϕ_t	ϕ_c	ϕ_t	–	ϕ_t	ϕ_c	1
13	$(V_{bat} + V_s) \times 0.75$	ϕ_c	ϕ_t	ϕ_t	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	ϕ_c

Working principle of the converter: From Table 1 for state 6, S_{b1}, S_{b4}, S_{b8}, and S_{b9} are connected in phase 1 (ϕ_c) the charging phase and S_{b2}, S_{b3}, S_{b5}, S_{b6}, and S_{b7} are connected in phase 2 (ϕ_t) the discharging phase. In phase 1, the flying capacitors (C_{fly1} and C_{fly2}) are connected through the switches in series and share half the input voltage V_{bat} from the battery. In phase 2, the flying capacitors (C_{fly1} and C_{fly2}) are connected in parallel together with the second source V_s which can be fed from the solar if desired, delivers the load. To model the equivalent resistance R_{equ} in Fig. 1*b* which represents the complete model of the SCC to predict the output voltage, the reduced equivalent circuit of the converter for state 6 is developed in Fig. 2. The CMOS switch resistance is taken as r_{on} and the capacitor equivalent series resistance (ESR) is $resr_1$ and $resr_2$.

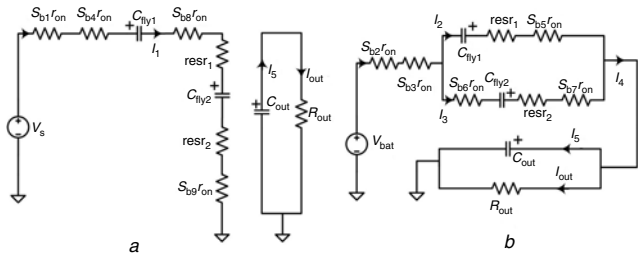

Fig. 2 *Equivalent circuit of series–parallel SCC*
a ϕ_c State
b ϕ_t State [2]

Theoretical framework: Theoretical analysis is performed on the SCC for the sixth state $(V_s + (V_{bat} \times 0.5))$ of Table 1 by utilising two different independent sources. The charging and discharging phase paths are shown by the firm and dotted lines in Fig. 1*a*. A similar analysis can be considered for other VCRs mentioned in Table 1. Evzelman *et al.* [3] have proposed an average current-based conduction loss model to develop R_{equ}. This analysis is derived from the basic circuit theory concept of approximating the SCC circuit in any operating phase to a first-order RC network. During a time period corresponding to a switching frequency, if charging and discharging processes in C_{fly1} and C_{fly2} are completed then the transition state is fully charge or slow switching limit and this occurs when the switching frequency is small or time period is large. On the contrary, if the switching frequency is large, then the time period is small the flying capacitors cannot completely charge and is said to be in the zero charge or fast switching limit mode where the current is constant in C_{fly1} and C_{fly2} [1, 3]. The average capacitor current in ϕ_c and ϕ_t is mapped to the I_{out}, given by [2, 3], where R_{equ} referred in Fig. 1*b* is the sum of the equivalent resistance defined by both the charge and discharge phases. Fig. 2 shows the equivalent circuit of the SCC

$$P_{equi} = I_{out}^2 R_{equi}. \tag{1}$$

If T_{ϕ_c} and T_{ϕ_t} are the time period during the ϕ_c and ϕ_t, then

$$\lambda_{\phi_c} = \left[\left(T_{\phi_c}/\left(4s_{b\phi_c} * r_{d(on)} + 2esr_{\phi_c}\right)\left(C_{fly}/2\right)\right)\right]/2, \tag{2}$$

$$\lambda_{\phi_t} = [(T_{\phi_t}/(3s_{b\phi_t} \times r_{d(on)} + esr_{\phi_t}/2) \times (2C_{fly} \times C_{out}/2C_{fly} + C_{out}))]/2, \tag{3}$$

During ϕ_c and ϕ_t to get R_{equ} the corresponding equivalent resistances are given as

$$R_{equ\phi_c} = \frac{0.125 \coth \lambda_{\phi_c}}{f_{switch} \times 0.5C_{fly}}, \tag{4}$$

$$R_{equ\phi_t} = \frac{0.5 \coth \lambda_{\phi_t}}{f_{switch}((2C_{fly} \times C_{out})/(2C_{fly} + C_{out}))}. \tag{5}$$

By combining and approximating (4) and (5), the R_{equ} of the converter is

$$R_{equ} = \frac{1}{4f_{switch} \times C_{fly}}\left[\coth\left(\lambda_{\phi_c}\right) + \coth\left(\lambda_{\phi_t}\right)\right]. \tag{6}$$

Once R_{equ} is known V_{out} referred in Fig. 1*b* can be calculated since V_o, I_{out} and R_{out} are also known. The model derived R_{equ} and the calculated V_{out} for different frequencies are shown in Table 2. Both the source voltages are assumed same and are taken as 1.17 and 2 for 100 and 5 kHz, respectively.

Table 2: Modelling, simulation and hardware comparison for sixth state

f_{switch} kHz	λ_{ϕ_c}	λ_{ϕ_t}	R_{equ}	V_{out} model	V_{out} simulation	V_{out} hardware	η Hardware
100 (source = 1.17 V)	3.24	1.43	0.25	1.75	1.75	1.74	99%
5 (source = 1.2 V)	1.62	7.17	5	1.76	1.78	1.74	96.5%

Implementation and key results: For validation of the converter, the prototype developed is shown in Fig. 3. The switches S_{b1}–S_{b9} used are bi-directional SPST analogue switches manufactured by MAXIM INTEGRATED circuits MAX4678 with individual $r_{on} = 0.3\,\Omega$. The flying capacitor and filter capacitor are manufactured by SANYOUNG 22 µF, 50 V with an ESR of 100 mΩ. The load current ranges between 10 µA and 10 mA at an output voltage level of 0.55–2.5 V. Fig. 3*a* shows a prototype of the PIC16F controller which is used to generate a switching sequence for the CMOS switch and liquid-crystal display are used to display the particular state of the proposed converter. The dead time is 10 ns. Fig. 3*B* shows the MAX4678 SMD bidirectional switch and the prototype size is 5 cm × 5 cm including all components. Fig. 3*C* shows the test bench of the proposed prototype where a light emitting diode is used as a load which is highlighted in the circle. The experimental result shown in Fig. 3*D* corresponds to an input voltage of 1.17 V and the output voltage is 1.76 V which is in good agreement with state 6. Two frequencies 100 and 5 kHz with a duty cycle of 50% are implemented and shown in Fig. 4. We can conclude from Fig. 4 that for these frequencies, simulation, modelling and experimental results are in good agreement with each other as shown in Table 2. Fig. 5*a* shows the comparison of work in [2] with diode and the proposed topology in this Letter without diode. The efficiency increases considerably and is >90%. The size of the prototype is very much smaller than the size of the existing converter discussed in [2], with two more additional VCRs, is an additional feature of the proposed converter. Fig. 5*b* shows a comparison of the first 11 VCRs derived by the switching sequence referred in Table 1 for modelling, simulation and hardware results of the proposed circuit. For regulation, the first method is to change the VCRs by proper gating to get the corresponding voltage and the second method is to adopt a variable switching frequency to vary R_{equ} which in turn gives the desired output variable V_{out}. This can be verified in Table 2 as it is 1.74 for 1.17 V input with frequency 100 kHz against 1.74 for 1.2 V at 5 kHz. Fig. 6*a* shows the simulation, analysis and experimental results of states 12 and 13.

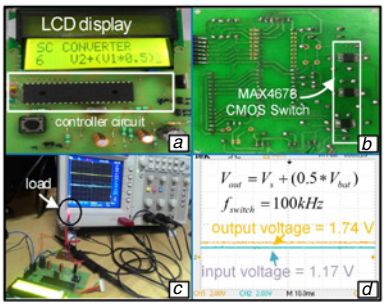

Fig. 3 *Hardware prototype*

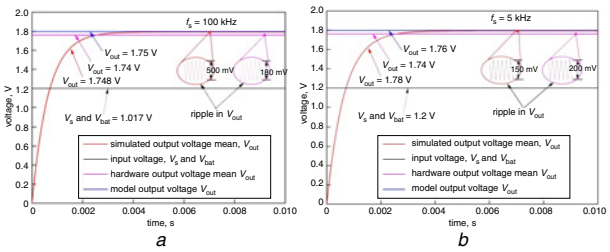

Fig. 4 *Simulation, analysis and experimental results for state 6 frequencies*

a 100 kHz
b 5 kHz

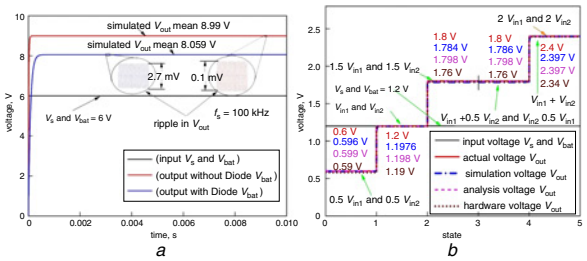

Fig. 5 *Comparison of simulated, modeled and experimental results*

a Output voltage with and without diode for input voltage of 6 V
b VCR comparison of all 13 states of proposed converter

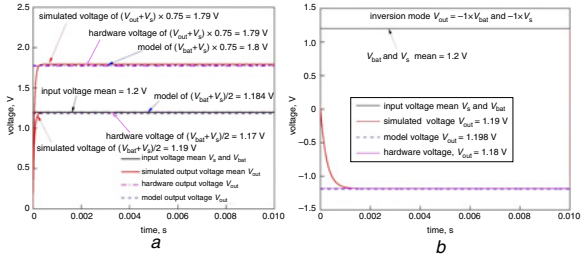

Fig. 6 *Simulation, analysis and experimental results*

a States 12 and 13
b States 14 and 15

Modified circuit of inversion mode: With the addition of one more switch S_{b10}, in between switches S_{b8} and S_{b6} of Fig. 1*a*, two more VCRs in the inversion mode [4] can be realised. The complete results are shown in Fig. 6*b*. The switching states are explained in Table 3 to realise the inversion mode.

Table 3: Inversion states

States	VCRs	S_{b1}	S_{b2}	S_{b3}	S_{b4}	S_{b5}	S_{b6}	S_{b7}	S_{b8}	S_{b9}	S_{b10}
14	$V_{bat} \times -1$	ϕ_c	–	ϕ_c	–	1	1	ϕ_t	ϕ_c	ϕ_t	ϕ_t
15	$V_s \times -1$	–	ϕ_c	ϕ_c	–	1	1	ϕ_t	ϕ_c	ϕ_t	ϕ_t

Conclusion and future work: A reconfigurable highly efficient CMOS-based dual input variable output buck boost SCC for low-power applications is proposed and verified in this Letter. The converter delivers high efficiency in an open loop with a significant increase in efficiency due to the reduced switch count, low weight and size, making it an excellent choice for on chip integration.

Submitted: *18 September 2017* E-first: *30 November 2017*
doi: 10.1049/el.2017.3576
One or more of the Figures in this Letter are available in colour online.

C. Abraham and B. R. Jose (*Division of Electronics, Cochin University of Science and Technology, Kochi, Kerala, India*)

✉ E-mail: chikkuabraham@yahoo.co.in

V. Subburaj, D. Jena and P. Perumal (*National Institute of Technology Karnataka, Surathkal, India*)

J. Mathew (*Department of Computer Science, Indian Institute of Technology Patna, Patna, Bihar, India*)

C. Abraham: Also with Muthoot Institute of Technology and Science, Kerala, India

References

1 Seeman, M.D., and Douglas, M.: 'A design methodology for SC DC–DC converters' (University of California, Berkeley, 2009)
2 Abraham, C., Jose, B.R., Mathew, J., *et al.*: 'Modelling, simulation and experimental investigation of a new two input, series-parallel SCC', *Power Electron.*, 2017, **10**, pp. 368–376
3 Evzelman, M., and Ben-Yaakov, S.: 'Average-current-based conduction losses model of SCC', *Trans. Power Electron.*, 2013, **28**, pp. 3341–3352
4 Abraham, C., Jose, B.R., Mathew, J., *et al.*: 'A dual input buck, boost and inverter mode SC based voltage converter'. Indian patent application no. 201741031722 filed on 2017/09/07