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Ultra-low voltage, power efficient continuous-time filters in 180 nm CMOS technology

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Abstract: The authors propose circuit techniques to implement integrated continuous-time filters for low voltage and low power applications. A fourth order G_m-C filter and a fifth order active-RC Chebyshev filter are used as test vehicles to validate the ideas. Basic building blocks are bulk driven transconductors. G_m-C filter and active-RC filter offer bandwidth of 1 MHz and 750 kHz, respectively while exhibiting a good figure of merit thus ensuring that the designs are energy efficient. Both the filters, fabricated on the same chip in 180 nm CMOS technology, operate on 0.5 V power supply. They offer a dynamic range of 45 and 46.6 dB, respectively.

1 Introduction

Semiconductor industries have witnessed the steady scaling down of technology for a couple of decades. Increased complexity, improved chip performance, and reduced power consumption [1] are some of the benefits of scaling of technology. Reliability issues dictate the supply voltages also to scale with device dimensions [2] approximately by the same factor. Further, lower power consumption requirements demand aggressive supply voltage scaling for a given technology node and more so in the case of digital circuits to reduce dynamic power consumption. However, in a typical system-on-chip (SoC) where analogue and radio frequency front end co-exist with the digital circuits for improved performance and power efficiency [3], analogue circuits are forced to work with low power supplies. With an increased number of applications, SoC designs have become very complex and low power is a mandatory requirement. Although scaling has resulted in improved performance in digital circuits, analogue designs benefit only marginally, as minimum-sized transistors suffer from noise and offset problems. It is a real challenge for analogue designers to design efficient analogue circuits to satisfy low power requirements without compromising on the dynamic range [4]. In the present day technology, analogue front-end is present in almost all SoCs, which are used for processing real-world signals [5].

It is an observed trend that, with technology scaling, the threshold voltage (V_{TH}) of a metal oxide semiconductor field effect transistor (MOSFET) does not scale with the same proportion as the power supply voltage does [6, 7]. This is indeed due to a design decision where the primary reason is to keep the sub-threshold currents [5] and noise margins in check. At supply voltages below 1 V, it is challenging to design CMOS analogue circuits using standard analogue design techniques, as the transistors fail to operate in strong inversion. Both the negative channel metal oxide semiconductor (NMOS) and positive channel metal oxide semiconductor (PMOS) require a gate to source voltage (V_{GS}) of at least one V_{TH} in order to be biased in moderate inversion. To meet this requirement, a supply voltage of atleast 2 V_{TH} is needed [8].

In order to cope up with the aggressive power supply reduction requirement of digital blocks [9, 10], many analogue circuit techniques have been reported in the literature such as voltage boosting [11], floating gate approach [9, 12], using the bulk driven weakly inverted devices [13–15] etc. to address the issues involved with low supply voltage and relatively higher V_{TH}. Voltage boosting circuits are effective only for light/negligible load applications as far as speed and power are concerned. The circuits become complex as the load increases. In addition, this technique is prone to ripple and the resulting switching noise can have a serious effect on the performance of analogue circuits which the voltage booster powers. Floating gate approach is an effective method where the V_{TH} of the MOSFET is tuned using multiple inputs to the floating gate. However, the output impedance of a floating gate transistor is lower, hence, the achievable gain will be lower. Further, this technique requires additional process steps for fabricating floating gates and hence results in increased cost. In the bulk driven technique, the signal is applied to the bulk-terminal of the transistor which modulates the current flow through the transistor, whereas biasing is done through the gate of the device. With this approach, it is possible to have both positive and negative bias voltages (body-source voltage V_{BS}) for the devices thus offering tunability of V_{TH}. A small forward bias of source–body junction would reduce $|V_{TH}|$ of the transistor. This increases the achievable signal swing which would help to increase the dynamic range of the circuit. The concept of body biasing was found to be useful for low voltage digital circuits [16, 17]. In analogue circuits, this concept was proposed by Guzinski *et al*. [18] in 1987 wherein a bulk driven operational transconductance amplifier (OTA) was proposed. The research thereon led to many analogue circuits such as transconductors, filters, phase-locked loops (PLLs) etc. at sub-1 V power supply. A break-through work by Chatterjee *et al*., in [13] is an example of realising continuous-time filters using 0.5 V supply voltage.

An integrator, being the building block of any continuous-time filter, can be realised either by active-RC or by transconductor–capacitor (G_m-C) structures. Active-RC approach has better linearity and dynamic range over G_m-C filter configuration for a given power dissipation due to its closed loop operation. It can be realised using operational amplifiers (op-amps) or OTAs. OTAs are attractive when compared to op-amps as the latter demands a large power for their low resistance output stage [19, 20]. However, OTAs can only be used with a careful design as outlined in [20]. One of the demerits of active-RC filters is that they are slow when compared to G_m-C filters because of their closed-loop structure. The conventional Miller compensation used to stabilise the loop makes the system even slower owing to the charging/discharging time of the compensating capacitor. Increase in the speed can be achieved only at the expense of increased gain–bandwidth product of the OTA which in-turn demands increased power. The requirement of large gain–bandwidth product for the OTA has been

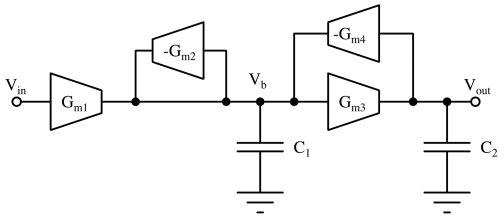


Fig. 1 *Second order G_m-C low-pass filter*

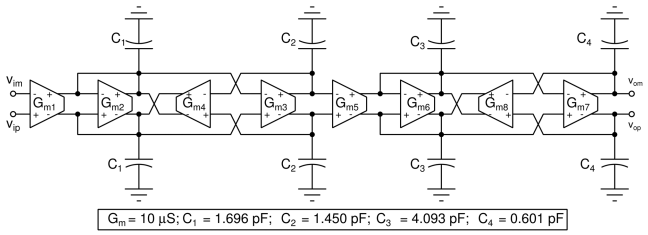


Fig. 2 *Fully differential fourth order G_m-C low-pass filter architecture*

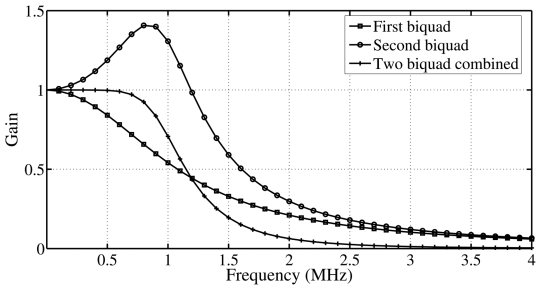


Fig. 3 *Response of fourth order G_m-C low-pass filter*

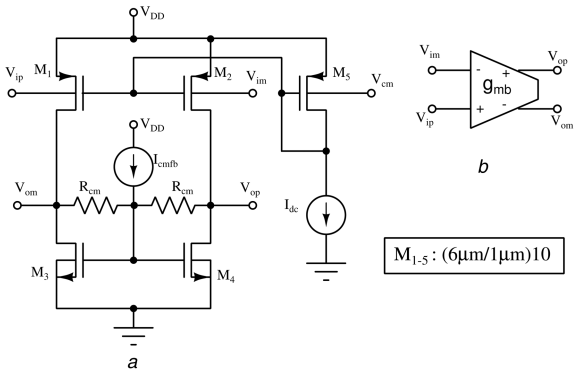


Fig. 4 *Bulk-driven pseudo-differential transconductor*
(a) Schematic, **(b)** Symbol

an impediment for pushing the bandwidth of the filter (realised using such OTAs) to its limits for a given power.

In this work, both an active-RC and a G_m-C filter operating on 0.5 V supply are implemented on silicon in 180 nm standard CMOS technology. The basic building block of such filters is bulk driven transconductor. These filters with bandwidths ranging from few kHz to MHz find applications as anti-aliasing filters and filters used in wireless communication. Rest of this paper is organised as follows. Section 2 gives the design of the fourth order G_m-C filter with common-mode feedback (CMFB) circuit. Section 3 discusses the design of a fifth order active-RC filter. State space modelling and design centering the filter are discussed in brief in Section 4. Test setup for the characterisation of the fabricated chip is explained in Section 5. Results are discussed in Section 6. Conclusions are drawn in Section 7.

2 Fourth order G_m-C filter

A fourth order G_m-C filter can be realised by cascading two second-order sections [21, 22]. A second order G_m-C low-pass filter is shown in Fig. 1 and is characterised by the transfer function as shown in (1) [23].

$$\frac{V_{out}}{V_{in}} = \frac{G_{m1}/G_{m4}}{[C_1C_2/G_{m3}G_{m4}]s^2 + [G_{m2}C_2/G_{m3}G_{m4}]s + 1} \tag{1}$$

DC gain, pole frequency (ω_o) and quality factor (Q) of the filter are given by the following

$$\text{DC gain} = \frac{G_{m1}}{G_{m4}} \tag{2}$$

$$\omega_o = \sqrt{\frac{G_{m3}G_{m4}}{C_1C_2}} \tag{3}$$

$$Q = \sqrt{\frac{G_{m3}G_{m4}}{G_{m2}^2}\frac{C_1}{C_2}} \tag{4}$$

It is clear from these equations that the filter can be tuned for the desired DC gain, ω_o and Q by a proper choice of transconductances and capacitances. If all transconductances are equal (say G_m), then DC gain, ω_o and Q can be written as follows:

$$\text{DC gain} = 1 \tag{5}$$

$$\omega_o = \frac{G_m}{\sqrt{C_1C_2}} \tag{6}$$

$$Q = \sqrt{\frac{C_1}{C_2}} \tag{7}$$

Fourth order low-pass Butterworth filter is realised by connecting two second-order sections in cascade as shown in Fig. 2. This figure shows the fully differential architecture as the transconductors designed in this work are fully differential.

Pole frequency f_o and Q of individual sections required to obtain the Butterworth response having a desired 3 dB bandwidth ($f_{-3\,\text{dB}}$) for a fourth order filter are obtained from the filter table [24]. f_o and Q of individual sections for $f_{-3\,\text{dB}} = 1$ MHz can be listed as follows:

- First second order section: $f_{o1} = 1$ MHz; $Q_1 = 0.541$.
- Second second order section: $f_{o2} = 1$ MHz; $Q_2 = 1.306$.

These second order sections are arranged in ascending order of Q in order to avoid the possible loss of dynamic range due to signal clipping if the high-Q section is placed first in the signal chain. In Fig. 2, all the transconductors are assumed to be equal having a transconductance of 10 µS. Accordingly, the capacitor values are computed for $f_{-3\,\text{dB}} = 1$ MHz and are given in this figure. Fig. 3 shows the response of this ideal filter along with the response of individual second order sections. Design of the proposed transconductor used to build this filter is explained in the next section.

2.1 Pseudo-differential bulk driven transconductor for G_m-C filter

Due to the limitations on overhead, low power supply transconductor circuits are forced to have a pseudo differential architecture [25]. Fig. 4 shows the designed pseudo differential transconductor with bulk driven inputs [21, 22]. v_{ip} and v_{im} are the differential inputs and v_{op} and v_{om} are the differential outputs. M_1 and M_2 are the PMOS input transistors and are sized to offer a bulk-transconductance of 10 µS when carrying a current of 2 µA. The gates of these transistors are biased to carry the required quiescent current, i.e. 2 µA through a current mirror transistor M_5. The input common-mode of the transconductor is chosen to be 0.25 V, i.e. $V_{DD}/2$. Transistors M_3 and M_4 form the NMOS current source loads and they operate in sub-threshold region. The gate

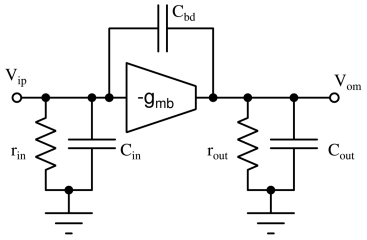


Fig. 5 *Single-ended small-signal equivalent circuit of the transconductor*

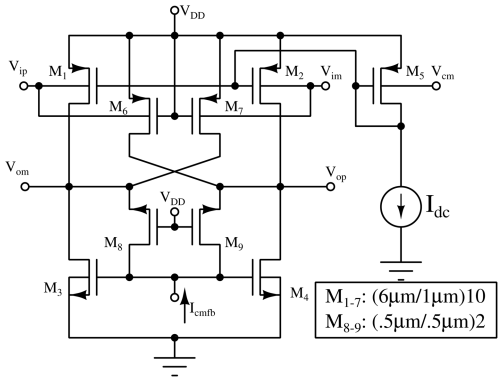


Fig. 6 *Complete schematic of the bulk-driven transconductor*

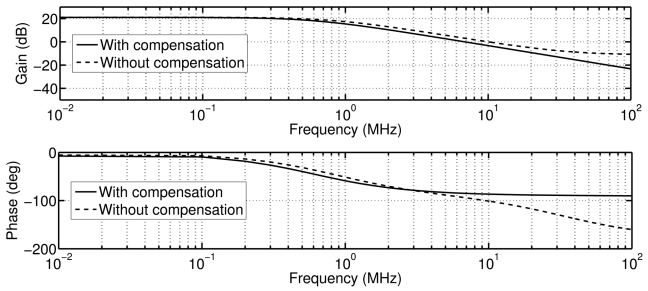


Fig. 7 *Frequency response of transconductor with and without compensation for right-half s-plane zero*

terminal of these transistors is biased by a CMFB which sets the output common mode of the transconductor to 0.25 V. The drain current of NMOS transistor operating in sub-threshold region as a function of gate to source voltage (V_{GS}) and drain to source voltage (V_{DS}) is given in (8) [26].

$$I_{DS} = \mu C_{ox}\frac{W}{L}(m-1)V_T^2 e^{(V_{GS}-V_{TH})/(mV_T)}(1-e^{-V_{DS}/V_T}) \tag{8}$$

where μ, C_{ox}, m, V_T ($= KT/q$) and V_{TH} are the mobility of the electron, capacitance per unit area presented by the gate oxide, sub-threshold slope factor, thermal voltage, and threshold voltage of the transistor, respectively. In (8), the drain current can be assumed to be independent of V_{DS}, i.e. $(1-e^{-V_{DS}/V_T}) \approx 1$, if V_{DS} is about 4–5 times more than V_T. The drain–source voltage (V_{DS}) of M_3 and M_4 (in Fig. 4) is at output common-mode voltage ($V_{DS,3,4} = 250\,\text{mV}$). Hence the above assumption is valid and the drain current can be assumed to be independent of V_{DS}. I_{DS} remains constant for a given V_{GS} and therefore, NMOS transistors M_3 and M_4 act as current source loads. The resistance R_{cm} and current source I_{cmfb} are part of the CMFB circuit and act as level shifter [13] to set the gate bias required for NMOS current source load. A careful look at the circuit reveals that there exists a parasitic capacitance between the input and output terminals of the transconductor. This is due to the body–drain junction capacitance of the PMOS input transistors, i.e. C_{bd} of M_1 appearing between v_{ip} and v_{om} and similarly, C_{bd} of M_2 appearing between v_{im} and v_{op}. These capacitances introduce a right half s-plane zero to the voltage transfer function of the transconductor. A single-ended small-signal equivalent circuit of

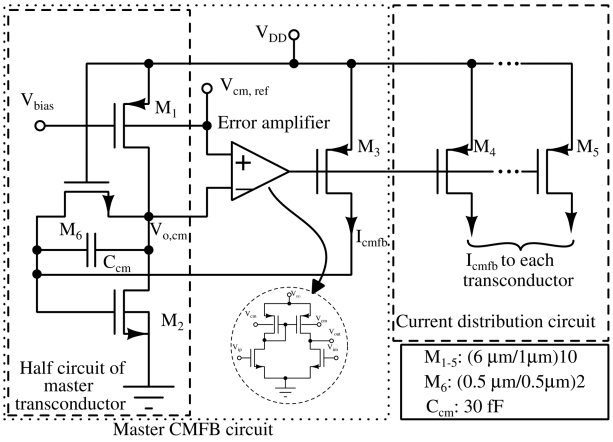


Fig. 8 *Schematic representation of common-mode feedback circuit*

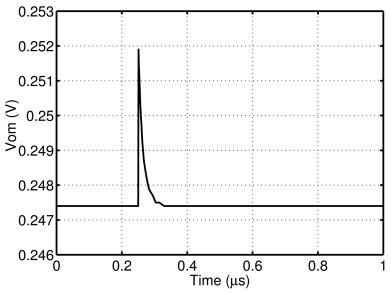


Fig. 9 *Response of transconductor to common-mode current impulse*

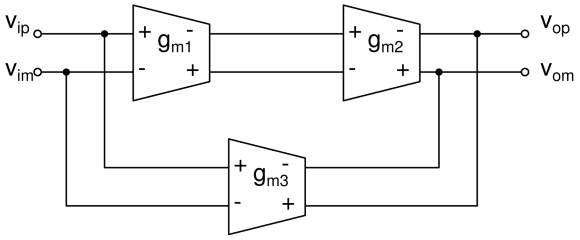


Fig. 10 *Block schematic representation of fully differential feed-forward compensated OTA*

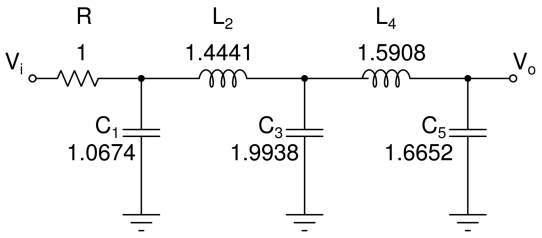


Fig. 11 *Prototype of LC ladder fifth order Chebyshev filter*

the transconductor is shown in Fig. 5. In the figure, g_{mb} is the transconductance of the input bulk driven transistor M_1 or M_2. C_{in} and C_{out} are the effective parasitic capacitances at the input and output, respectively. r_{in} and r_{out} are the effective input and output resistances. C_{bd} is the effective body–drain junction capacitance. Voltage transfer function of the differential transconductor can be written as

$$\frac{V_{op}-V_{om}}{V_{ip}-V_{im}} = \frac{g_{mb}r_{out}[1-(C_{bd}/g_{mb})s]}{1+r_{out}(C_{out}+C_{bd})s} \tag{9}$$

It is seen from (9) that there exists a right half s-plane zero at $s = g_{mb}/C_{bd}$ and this zero causes the frequency response to deviate from the ideal for frequencies beyond g_{mb}/C_{bd} rad/s. A simple scheme to compensate for the effect of right half s-plane zero is shown in Fig. 6. For a fully differential transconductor, v_{ip} and v_{im}

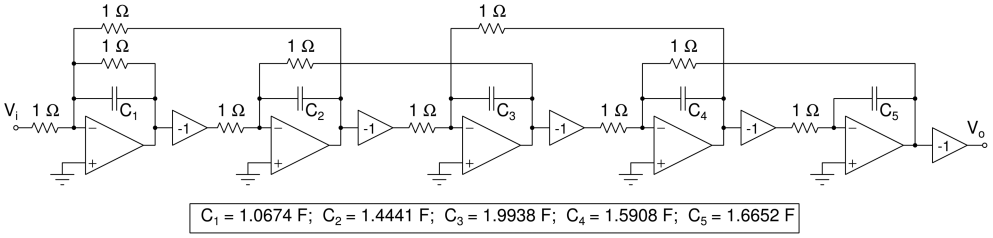


Fig. 12 *Singly terminated fifth order Active-RC ladder filter*

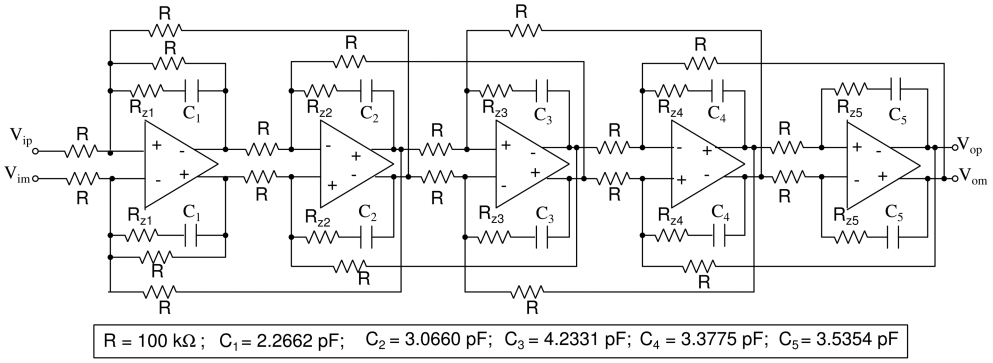


Fig. 13 *Schematic representation of the fully differential fifth order active-RC Chebyshev filter*

are equal in magnitude and out of phase; similarly v_{op} and v_{om}. This feature has been exploited in the compensating scheme by using two cross-connected PMOS dummy transistors M_6 and M_7. C_{bd} of M_6 tend to cancel any coupling between the v_{ip} and v_{om} that occurs due to C_{bd} of M_1. Similarly, M_7 compensates for C_{bd} of M_2. These dummy transistors do not take any active part in transcondutor action. It is to be noted that this scheme will only compensate for the capacitance but will not cancel the effect of capacitor altogether. To justify the effect of the proposed scheme, frequency response of the transconductor is plotted in Fig. 7 without and with compensation. It is evident from the figure that the transconductor with compensation offers a first order response with a roll-off of −20 dB per decade. Without the compensation, the phase lag exceeds 90° (excess phase) and the magnitude response is pulled upwards beyond frequency of 3 MHz, thus clearly indicating the effect of right half *s*-plane zero. The phase response of the compensated transconductor tends to −90° at higher frequencies. It is also observed that the compensation scheme reduces the effective bandwidth of the transconductor. This is expected since the PMOS transistors M_6 and M_7 increase the effective capacitance at the output nodes v_{op} and v_{om}, respectively. Resistors R_{cm} shown in Fig. 4 are realised by using the NMOS transistors as shown in Fig. 6. The NMOS transistors M_8 and M_9 are used to realise R_{cm} and they operate in subthreshold region. They are sized to offer high resistance of the order of few hundreds of mega ohms so that they do not load the transconductor differentially.

2.2 CMFB circuit

In G_m-C filters, output of one transconductor drives the input of another transconductor. Therefore, it is common to set the output common-mode DC voltage of the transconductor equal to the input common-mode DC voltage. Further, to maximise the swing, input, and output common-mode voltages are set to $V_{DD}/2$. A master–slave circuit arrangement has been used in this work [22], to set the output common-mode voltage of transconductor. The master circuit sets the common mode of a master transconductor using a negative feedback loop. The so generated tuning current is distributed to all the transconductors of the filter through current distribution circuit. The schematic representation of the master CMFB circuit is shown in Fig. 8. Transistors M_1, M_2, and M_6 form the master transconductor which is identical to the common-mode equivalent half circuit of the transconductor shown in Fig. 6. The output common-mode DC voltage of the master transconductor is sensed and compared with the reference common-mode voltage ($V_{cm,ref}$) by the error amplifier. This error amplifier is chosen to be a gate driven NMOS input pseudo-differential amplifier as it drives the gates of PMOS current sources whose voltages are referenced to V_{DD}. The negative feedback loop sets the current I_{cmfb} such that the output common-mode voltage ($V_{o,cm}$) is made equal to the reference voltage ($V_{cm,ref}$). The resulting I_{cmfb} is distributed to all the transconductors using current distribution circuit. The capacitor C_{cm} is used in parallel with M_6 to improve the stability of the common-mode loop. Fig. 9 shows the response of common-mode loop for a common-mode disturbance (common-mode current impulse of 2 μA for a duration of 1 ns). The loop is found to be stable.

3 Fifth order active-RC Chebyshev filter

In the case of active-RC filter, the DC gain of the OTA must be as high as possible to get a good filter response [27]. To achieve this, transconductors are cascaded necessitating a compensation for stable operation when used in a closed loop. Use of conventional Miller compensation is found to degrade the gain–bandwidth product of the OTA. This limitation can be overcome by using a feedforward frequency compensation technique [28] which pushes the gain–bandwidth product of the OTA to a higher value [29]. It also improves the phase margin of the OTA without compromising the bandwidth [30–32]. A feed-forward OTA is designed in this work using three transconductors [30–32] – two in the forward path and one in the feedforward path. The block schematic representation of the same is shown in Fig. 10. It is to be noted that DC gain enhancement of 73% was achieved by this feedforward structure. And also 3 dB bandwidth was improved by three times, for the same UGB when compared with the Miller compensated OTA [32]. A fifth-order Chebyshev low pass filter is realised using the designed feedforward compensated OTAs. The filter is derived from the singly terminated LC ladder architecture whose prototype is shown in Fig. 11 [33]. The element values shown are for 1 Ω terminating resistance and a band edge of 1 rad/s. An active-RC realisation of the prototype LC ladder can be derived by first converting the LC ladder into a G_m-C filter which in turn is achieved by emulating inductors using gyrator–capacitor architecture. The so obtaining G_m-C filter is then converted into an equivalent active-RC filter. Singly terminated active-RC ladder filter prototype is shown in Fig. 12. In this figure, all resistors are of value 1 Ω. Capacitors C_1, C_3, and C_5 have same values as shown in Fig. 11. The values of capacitors C_2 and C_4 are same as that of L_2

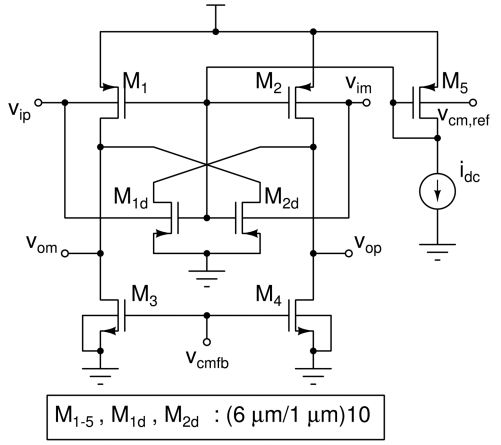


Fig. 14 *Pseudo-differential transconductor for active-RC filter*

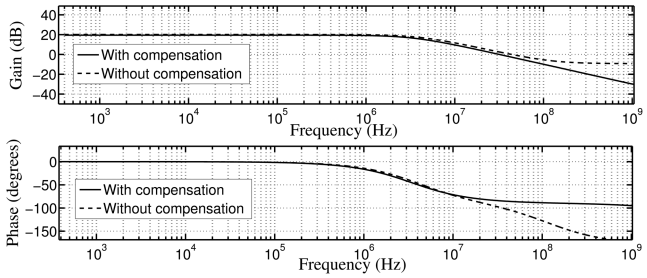


Fig. 15 *Frequency response of transconductor with and without the proposed scheme for compensating for the effect of* C_{bd}

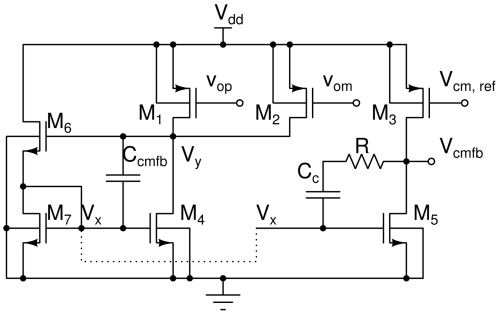


Fig. 16 *Schematic representation of CMFB circuit*

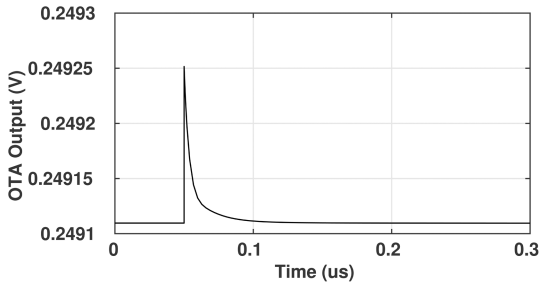


Fig. 17 *Response of the OTA for common-mode perturbation*

and L_4 in Fig. 11, i.e. $C_2 = 1.4441$ F and $C_4 = 1.5908$ F. This active-RC prototype filter is then scaled to the desired terminating resistance and cut-off frequency. The filter is chosen to have a band edge of 750 kHz. The band edge of the ladder filter is well below the 3 dB bandwidth of the OTA. The terminating resistance is chosen to be 100 kΩ. It is chosen such that after scaling, the desired capacitance values are <10 pF. Due to its inherent merits, a fully differential architecture of the filter is realised in this work as shown in Fig. 13. In this circuit, resistors R_{zi} are used to eliminate the effect of right half $s-$ plane zero resulting from using OTAs instead of Opamps. Further, node scaling is done on the filter to maximise the dynamic range.

3.1 Pseudo-differential bulk driven transconductor for active-RC filter

A pseudo-differential bulk driven transconductor used to realise the feedforward OTA and hence the active-RC filter is shown in Fig. 14. PMOS input transistors are sized to offer a bulk transconductance of 40 μS when carrying a current of 10 μA. The gates of these transistors are biased to carry the required quiescent current, i.e. 10 μA through a current mirror transistor M_5. A similar single-ended small-signal equivalent circuit can be derived for this transconductor too, as we did in the previous case (Fig. 5). To compensate for the effect of right half s-plane zero (at g_{mb}/C_{bd}) because of body–drain junction capacitance, two dummy transistors M_{1d} and M_{2d} are connected between v_{ip} and v_{op} and v_{im} and v_{om} as shown. Fig. 15 shows the frequency response of the transconductor with and without the compensation. A separate CMFB circuit is designed for this transconductor [32] and is briefly discussed in the next section.

3.2 CMFB circuit

The filter architecture demands the input and output common-mode voltages of the OTAs to be maintained at the same value so that the OTAs are not loaded when in DC bias condition. Therefore, output of each OTA is set to a voltage equal to a reference voltage. A CMFB circuit is commonly used for this purpose. For the feed-forward OTA used in this filter, there are two stages built using three pseudo differential transconductors (refer Fig. 10). The OTA requires only two CMFB circuits. First CMFB circuit is used for the first stage transconductor. Second CMFB circuit is used for the second stage transconductor and the feed-forward transconductor as their outputs are common. Fig. 16 shows the CMFB circuit used for the transconductor. In the figure, v_{om} and v_{op} are the inputs to the CMFB circuit which come from the outputs of the transconductor. The transistors M_1 and M_2 operate in weak inversion and they convert the output common-mode voltage into currents. The sum of the drain currents of M_1 and M_2 is sensitive only to the output common-mode voltage of the transconductor. Transistor M_3 is driven by the common-mode reference voltage ($V_{cm,ref}$). The size of this transistor is made double of that of M_1 and M_2 so that the drain current of it equals the sum of drain currents of M_1 and M_2. The transistors M_6 and M_7 together generate a voltage V_x that biases the transistor M_4 to carry current exactly equal to the sum of drain currents of M_1 and M_2. Since the gate of the transistor M_5 is also biased with the same V_x, M_5 also carries a current equal to that of M_4. Thus the drain current of M_5 carries the common-mode information. At the node V_{cmfb} (output node of the CMFB circuit), the drain current of M_3 is compared with that of M_5. Any error between them, will generate a voltage V_{cmfb} which biases the NMOS loads of the transconductor (refer Fig. 14), thus closing the loop. The negative feedback loop will act in such a way as to make the output common-mode voltage of the transconductor equal to the common-mode reference voltage $V_{cm,ref}$. The capacitors C_{cmfb}, C_c, and the resistor R are used to stabilise the negative feedback loop against common-mode perturbations. The response of the OTA for the common-mode perturbation is shown in Fig. 17. Response settles down to common-mode value at around 50 ns.

A careful look at Fig. 16 reveals that we can achieve the same functionality with a simple current mirror load using the transistors M_4 and M_5. However, this mirroring suffers from serious channel length modulation effect especially operating at 0.5 V supply, since the V_{cmfb} is of the order of 360 mV. Hence, the transistors M_6 and M_7 are used, with careful sizing, to ensure that the drain potential of M_4 and M_5 are atleast near equal, if not equal.

Fig. 18 shows the DC input–output characteristic of feed-forward OTA. It shows the effect of CMFB circuit on the linearity of the OTA and hence the transconductor.

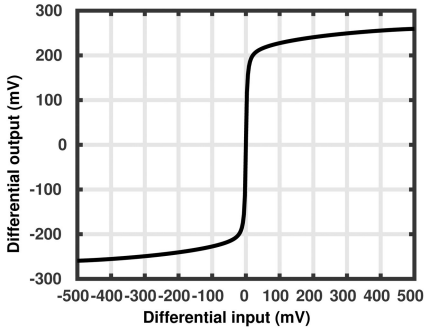


Fig. 18 *DC input–output characteristic of feed-forward OTA*

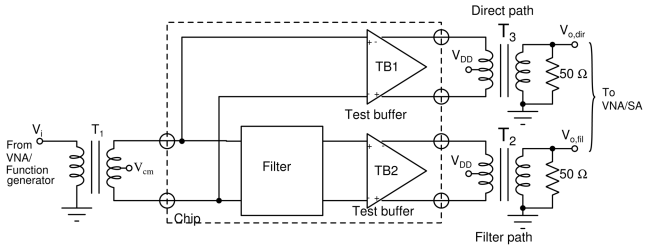


Fig. 19 *Test set-up for on-chip filter characterisation*

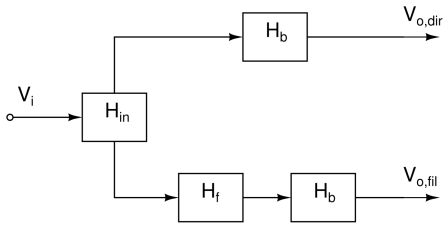


Fig. 20 *Block diagram of the test setup*

4 State space modelling and design centering of the filters

Non-idealities of the OTA and interconnect parasitics cause the frequency response to deviate from the ideal response. Design centering is done on the filter in order to bring back the filter response to ideal. In [34], a design centering technique for G_m-C filters has been proposed based on the space mapping method. Here, the filter is optimised in a model space of the filter and the results are interpreted in actual filter space. Such a method has been followed for design centering the filters designed in this work too [32]. The space mapping technique demands the filter to be modelled. Higher the accuracy of the model, fewer will be the number of design centering iterations. State space model is a good choice since the filter can be modelled easily and the MATLAB tool can be used effectively for optimising the filter in model space. Hence the filter is modelled using state equations in this work. MATLAB built-in optimisation routine, *fminsearch* is used to minimise the error between the frequency response of state space model and that of the ideal by tuning the integrating capacitors and resistors. Optimised values of resistors and capacitors are then used in the transistor level filter. If the model is accurate, the optimised component values when put in actual filter would give a response close to ideal. This tuning is done once after the schematic design to eliminate the effect of OTA parasitics and then again done after the layout to minimise the effects of interconnect parasitics.

5 Test setup

Characterisation of integrated continuous-time filters requires the filter output signal to be brought out of the chip for measurements. However, typically, the filters are not designed to drive large capacitive loads offered by the IC package or the 50 Ω load offered by the measuring instruments such as vector network analyser (VNA)/spectrum analyser (SA). It is common to use buffers to drive such large loads. However, when characterising the filter in packaged chips, effects of the test buffers and the package parasitics must be de-embedded from the filter response. A simple technique is proposed in [27] to characterise packaged integrated filters. This technique is accurate enough for characterising low-frequency filters where the package parasitics can be considered to have negligible effect on the measured stop-band characteristic of the filter. For the filters designed in this work, this approach has been used. Fig. 19 shows the test-setup used for characterising the fabricated filters.

The filter to be tested is assumed to be fully differential. Transformer T_1 converts the single-ended excitation from the test equipment into a fully differential signal to be fed to the filter differential inputs. Since the filter is not designed to drive the external loads, two nominally identical on-chip test buffers TB1 and TB2 are used. These test buffers are biased by sufficiently large currents so that they are able to drive the external loads. They are activated only during characterisation. TB1 senses the input of the filter and forms the direct measurement path while TB2 senses the output of the filter and forms the filter measurement path. Transformers T_2 and T_3 convert the test buffer outputs into single-ended signals that are measured by the test instruments. The test buffers, IC package, and board parasitics have a frequency response that must be de-embedded in order to obtain the true filter response. While characterisation, it is assumed that both the test buffers are matched and their input resistances are negligible. The block diagram representation of the test set-up is shown in Fig. 20.

H_{in} is the transfer function of the input path, i.e. from v_i to the input of the filter. H_f is the filter transfer function and H_b is the transfer function from the test buffer input to the final output (outputs of T_2 and T_3 in Fig. 19). From the block diagram, the frequency response of the filter can be written as

$$H_{\rm f}(f) = \frac{V_{o,\rm fil}(f)}{V_{o,\rm dir}(f)} \tag{10}$$

SA or VNA can be used to measure $H_f(f)$. If magnitude response is only of interest, SA can be used to measure $V_{o,\rm fil}(f)$ and $V_{o,\rm dir}(f)$ independently and $H_f(f)$ can be computed from $V_{o,\rm fil}(f)$ and $V_{o,\rm dir}(f)$. If VNA is used for measurements, S-parameters of the filter path and the direct path can be measured from which the filter response can be obtained. Assuming a good impedance match, it can be shown that

$$H_{\rm f}(f) = \frac{V_{o,\rm fil}(f)}{V_{o,\rm dir}(f)} = \frac{S_{21,\rm fil}(f)}{S_{21,\rm dir}(f)} \tag{11}$$

5.1 Test buffer design

Fig. 21 shows the schematic representation of the test buffer designed to drive external loads. It is designed to operate on 3.3 V supply since linearity of buffer should be maintained at a level much higher than that of the filter. The buffer has fully differential architecture and has two stages. The first stage is a source follower formed by the input transistors M_1 and M_2, and the second is a differential amplifier (source-coupled differential pair) converting analogue output to a proportional current. The source follower stage serves two purposes. First, it offers a capacitive load to the filter. The sizes of the input transistors are made small so that they offer small capacitance and this small capacitance can be taken into account while design centering the filter. Second, the source follower acts as a level shifter raising the output common-mode DC of the filter (which is 0.25 V) to about 1.6 V such that the differential amplifier of the second stage will have sufficient headroom to offer the desired linearity. The differential amplifier is formed by the transistors M_3 and M_4 along with the tail-current source transistors M_5 and M_6. Transistors M_3 and M_4 are sized so that they have a large gate overdrive voltage while they are made to carry large currents of ∼15 mA. This is important because distortion of the test buffer must be small when compared to that introduced by the filter. However, since the filter is designed to work at a differential swing of 1 V peak-to-peak, the achievable gate overdrive is not sufficient to keep the distortion of the buffer

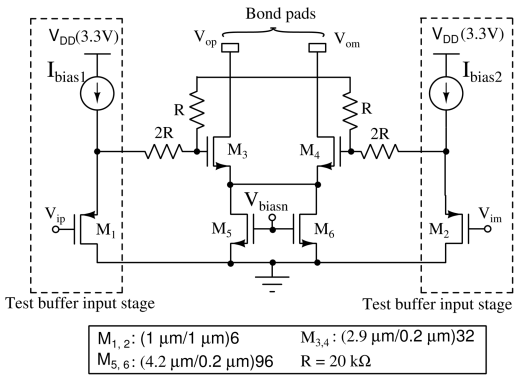


Fig. 21 *Schematic representation of test buffer*

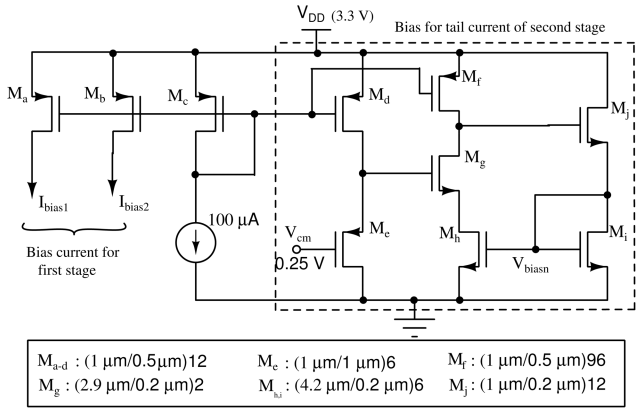
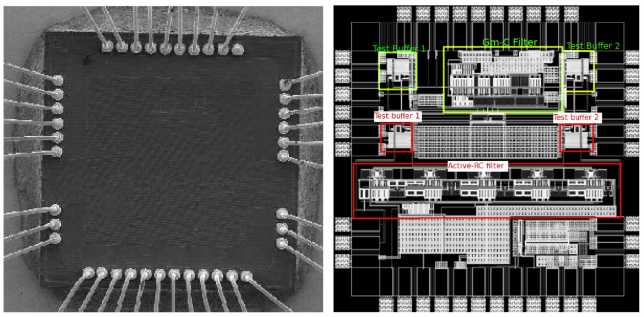


Fig. 22 *Biasing circuit for test buffer*



a *b*

Fig. 23 *Fabricated chip*
(a) Die photograph, ***(b)*** Snapshot of top-level layout of the chip

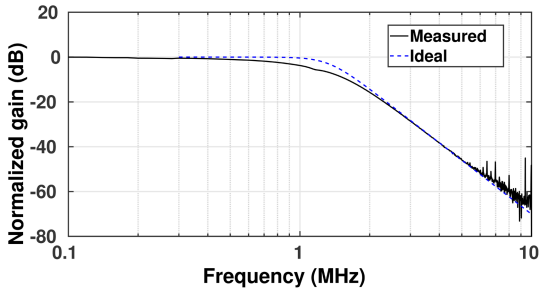


Fig. 24 *Normalised magnitude response of the G_m-C filter chip*

below the desired limits of −60 dB. Thus, to achieve the necessary buffer linearity, the output of the first stage is attenuated by a factor of three using a resistive potential divider, before feeding it to the next stage. Note that this potential divider is differential and hence operates only on output signal. Fig. 22 shows the biasing circuit used to bias the test buffers. An off-chip current of 100 μA, generated using the IC LM 334, is used as the reference. In Fig. 22, transistors M_a and M_b form the current sources (I_{bias1} and I_{bias2}, respectively) for the input stage of test-buffer circuit of Fig. 21. The bias voltage (V_{biasn}) for the tail-current source of the second stage of the test buffer is generated by transistors $M_c - M_j$.

6 Measurement results

Proposed filters are fabricated using UMC 180 nm CMOS process through Europractice. Resistors are realised using high-resistivity polyresistors and capacitors are realised using metal-insulator-metal capacitors. Size of the die is 1.5 mm × 1.5 mm (2.25 mm^2) of which G_m-C filter along with accessories occupies an area of 0.25 mm^2 and the active-RC filter occupies an area of 0.775 mm^2. The die-photograph and the top-level layout of the fabricated chip is shown in Fig. 23. G_m-C and active-RC filters are highlighted separately in the layout. The chip is packaged in a 44-pin J-leaded chip carrier package. Different power supplies (3.3 V for test buffers, 0.5 V for the power supply of the filters, and 0.25 V for the common-mode reference) are generated off-chip by using voltage regulator ICs and buffers.

6.1 Frequency response measurements

Fig. 24 shows the normalised magnitude response of the on-chip G_m-C filter. When compared with the ideal response, the actual filter response is found to be in deviation near the band edge. However, the stopband performance of the filter is in a close match to the ideal with 80 dB/decade roll-off as expected. Fig. 25 shows the magnitude response of the filter for 18 samples of the fabricated chip. Consistency in the responses of the filter samples justifies the good repeatability. Fig. 26 shows the measured magnitude response of the active-RC Chebyshev filter and is also compared with the ideal. Fig. 27 shows the frequency response of 18 samples of the fabricated IC. It is evident that the fabricated chips offer very good repeatability with a ±2% variation in the bandwidth.

6.2 Noise spectral density

Fig. 28 shows the output voltage noise spectral density of the G_m-C filter. The measured integrated output noise of the filter over the frequency range of 40 kHz to 1.1 MHz is 217.2 μV [root mean square (rms)]. The voltage noise spectral density measured at the output of the active-RC filter is plotted in Fig. 29. The rms output noise when integrated to 1 MHz is found to be 851 μV.

6.3 Distortion performance

The HD_3 as a function of input peak-to-peak (differential) voltage for the G_m-C filter is plotted in Fig. 30 for a fixed frequency of 330 kHz (f_o/3). The filter offers 1% HD_3 (−40 dB) for an input differential peak-to-peak voltage of 135 mV. Fig. 31 shows the HD_3 for active-RC filter. Here, the tone is selected to be 250 kHz so that filter will have the third harmonic component as the dominant harmonic at the output while the higher order harmonics are naturally rejected by the filter characteristics. Designed active-RC filter offers 1% HD_3 (−40 dB) for an input differential peak-to-peak voltage of 285 mV.

6.4 Performance parameters

The performance parameters of both the filters are summarised in Table 1. Both the filter designs are compared with some of the low-voltage filters (gate/bulk driven) found in the literature and the comparison is given in Table 2. All the filters that are compared here are realised on silicon. Note that, for G_m-C filters in [14, 35], the linearity has been measured for a tone at a frequency much below the bandwidth. At frequencies much below the filter bandwidth, the distortion offered by G_m-C filters is typically small since the distortion currents of the transconductors cancel each other [36]. Hence the linearty will be obviously better. The figure of merit (FOM) [33] used for the comparison as

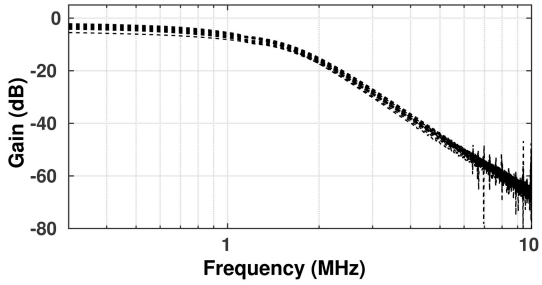


Fig. 25 *Magnitude response of 18 samples of fabricated G_m-C filter chips*

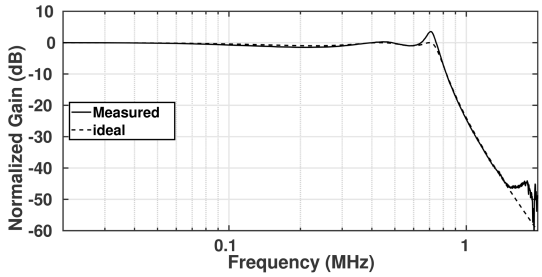


Fig. 26 *Normalised magnitude response of the Active-RC filter chip*

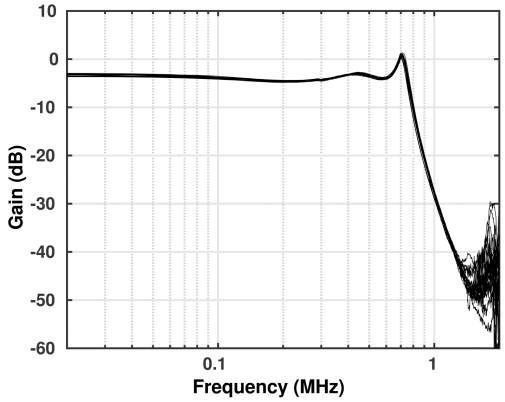


Fig. 27 *Magnitude response of 18 samples of fabricated active-RC filter chips*

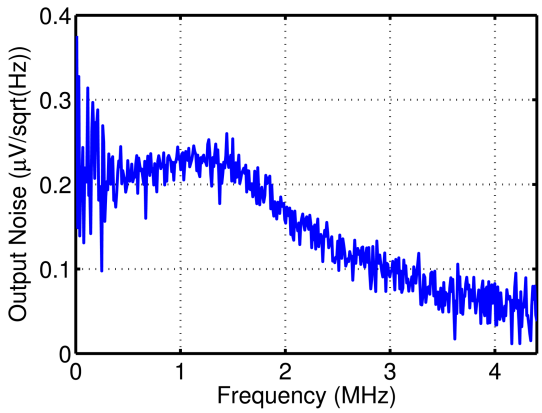


Fig. 28 *Measured output noise spectral density of G_m-C filter*

$$\text{FOM} = \frac{P_{\text{diss}}}{pQ_{\max} f_o \text{DR}^2} \tag{12}$$

where P_{diss} is the power dissipation, p is the number of filter poles, f_o is the filter cut-off frequency, $Q_{\max}$ is the maximum quality factor of the filter poles and DR is the dynamic range. A lower FOM indicates a more power efficient design. It is to be noted that there are a very few sub-1 V filters available in the literature that are realised on silicon.

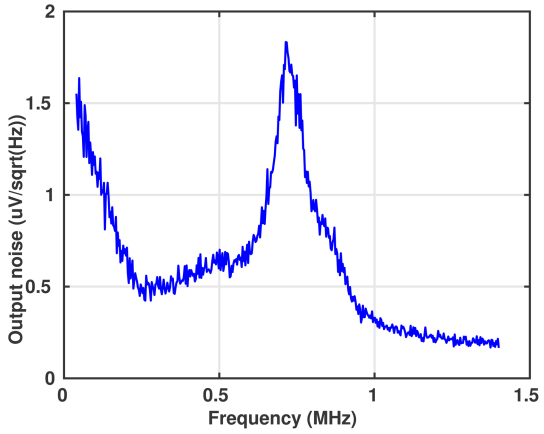


Fig. 29 *Measured output noise spectral density of active-RC filter*

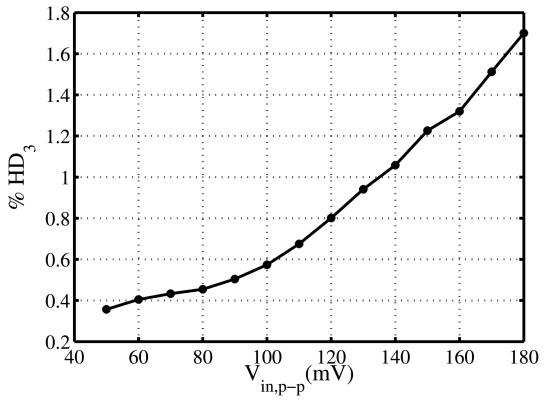


Fig. 30 HD_3 *versus input differential peak-to-peak voltage for a fixed frequency of 330 kHz for G_m-C filter*

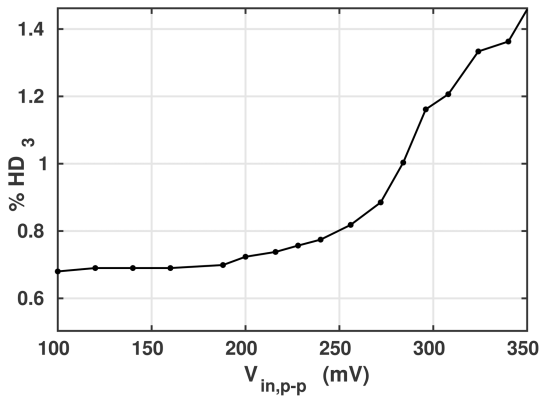


Fig. 31 HD_3 *versus input differential peak-to-peak voltage for a fixed frequency of 250 kHz for active-RC filter*

Table 1 Performance parameters of the filters

Parameters	G_m-C	Active-RC
supply voltage [V]	0.5	0.5
technology [nm]	180	180
3 dB bandwidth [MHz]	1.00	0.75
power dissipation [μW]	56.4	305.0
integrated output noise [μV rms]	217.22	851.00
$V_{\text{in}-\text{pp}}$ differential [mV]	192	768
for THD = −40 dB	—	—
dynamic range [dB]	45.00	46.33
for THD = −40 dB	—	—
area [mm^2]	0.125	0.650

Table 2 Comparison with some published filters

Reference	Bandwidth [MHz]	Order	Supply voltage [V]	Power [μW]	Q_{max}	Input [mV rms] for 1% THD	Dynamic range [dB] for THD ≅ −40 dB	Topology	Tech. [μm]	FOM (fJ)
[13]	0.135	5	0.5	1100[a]	6.2	50	56.6[b]	Active-RC	0.18	0.58
[14]	3	2	1.2	382	0.707	636.4	69.6[c]	G_m-C	0.35	0.009
[37]	1.05	3	1.8	4070	1.99	282.8	45[d]	G_m-C	0.18	20.53
[35]	0.010	2	1.5	648	0.707	166.1	62.6[e]	G_m-C	0.35	25.18
[38]	0.0175	2	1	44.3	0.71	530	63.7[f]	G_m-C	0.35	0.76
[39]	0.015	3	2.5	244	1.71	903	54.6[g]	G_m-C	0.35	10.99
[40]	5×10^{-5}	5	1	0.350	1.621	30	49.9	G_m-C	0.18	8.843
this work – G_m-C	1	4	0.5	56.4	1.3	67.89	45[h]	G_m-C	0.18	0.355
this work – active-RC	0.750	5	0.5	305	9.34	271.5	46.33[i]	active-RC	0.18	0.202

[a]Including the power for the PLL-based frequency tuning loop.
[b]Ratio of input at 100 kHz to integrated input noise for the range 1–150 kHz.
[c]Ratio of input at 1 kHz to integrated input noise for the range 100 Hz–4 MHz.
[d]Ratio of input at 1 MHz to integrated input noise for the range 1 Hz–1 MHz.
[e]Ratio of input at 1 kHz to integrated input noise for the range 10 Hz–10 kHz.
[f]Ratio of input at 1 kHz to integrated input noise for the range 1 Hz–18 kHz.
[g]Ratio of input at 1 kHz to integrated input noise for the range 100 Hz–15 kHz.
[h]Ratio of input at 750 kHz to integrated input noise for the range 40 kHz–1.1 MHz.
[i]Ratio of input at 550 kHz to integrated input noise for the range 40 kHz–1 MHz.

7 Conclusion

In this paper, ultra-low voltage, power efficient continuous-time filters are proposed. A fourth order G_m-C low pass filter having a cutoff frequency of 1 MHz and a fifth order Chebyshev Active-RC low pass filter having a cutoff frequency of 750 kHz are implemented on silicon in 180 nm standard CMOS technology with 0.5 V power supply. Filters use bulk driven transconductor as the building block. Active-RC filter uses a feedforward OTA (built by these bulk driven transconductors) to improve the gain–bandwidth product and stability. Operating on supply voltage <1 V, both the filters offer high bandwidth among the state-of-the-art filters reported in the literature. They also offer very low FOM indicating that the designs are power efficient.

8 Acknowledgments

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