MODELING, ANALYSIS AND OPTIMIZATION OF INTERCONNECTS IN DEEP SUBMICRON REGIME

Thesis
Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

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DECLARATION

by the Ph.D. Research Scholar

I hereby ***declare*** that the Research Thesis entitled **MODELING, ANALYSIS AND OPTIMIZATION OF INTERCONNECTS IN DEEP SUBMICRON REGIME** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirements for the award of the Degree of ***Doctor of Philosophy*** is a ***bona fide report of the research work carried out by me***. The material contained in this thesis has not been submitted to any University or Institution for the award of any degree.

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This is to *certify* that the Research Thesis entitled MODELING, ANALYSIS AND OPTIMIZATION OF INTERCONNECTS IN DEEP SUBMICRON REGIME, submitted by **Soorya Krishna K** (Register Number: EC07F02) as the record of the research work carried out by him, is *accepted* as the *Research Thesis submission* in partial fulfillment of the requirements for the award of degree of ***Doctor of Philosophy***.

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ABSTRACT

Integrated circuit technology is the base for all modern electronic systems. The development of modern integration technologies is normally driven by the needs of digital CMOS circuit design. Rapid progress in silicon VLSI technologies has made it possible to implement multi-function and high performance electronic circuits on a single die. This has led to the tremendous growth in integrated circuits technology resulting in highly complex circuits with increasing number of components and on-chip interconnects.

In digital domain, aggressive technology scaling redefines, in many ways, the role of interconnects vis-à-vis the logic in determining the overall performance. Although active devices mostly benefited from scaling, intermediate and global interconnects performance has degraded with scaling. Prominent reason being long interconnects do not scale with the technology. Apart from signal integrity, power dissipation and reliability issues, delays over long interconnects far exceeding the logic delay becomes a bottleneck in high speed operation. Moreover, with an increasing density of chips, the number of interchip connections is greatly increased as more and more functions are put on the same chip; thus, the size and performance of the chip are mostly dominated by wiring rather than devices.

This thesis addresses the issues associated with the on-chip long interconnects, namely, modeling, delay reduction , minimization of signal reflection at high frequencies at the interconnect-via junction and reducing the skew in clock signals. Design and analysis methodologies presented in this work focus on improving the performance of the interconnects in DSM regime.

Interconnects are represented by distributed RLGC networks and modeled using state space approach. Generalized state space matrices are derived for Single, Coupled,

L and **T** type of interconnects and these models are used to estimate interconnect metrics. Using the coupled interconnect models, crosstalk noise in the victim lines of the multi-coupled interconnects is estimated. Further, model order reduction using moment matching is employed to reduce the large order of the RLGC network to lower order for reducing the complexity of the network.

As an alternative to traditional repeater insertion method to reduce the intermediate/global interconnect delay, exploiting the resonant characteristics of the interconnects is gaining popularity. The idea of this method is to make a resonating interconnect by inserting an inductor of appropriate value along the interconnect to nullify the effect of interconnect parasitic capacitance. This scheme can be effectively used for clock signals as well as signal modulated data networks.

At high frequencies, impedance discontinuities at interconnect-via junction results in signal reflections and give rise to signal integrity problems. A methodology to minimize the via-induced signal reflections by the inclusion of an appropriate capacitive load is presented.

Clocks being the highest frequency signals in any IC, delay and skew of a few pico seconds in the transmitted clock signals is detrimental for the proper functioning of the circuit. Traditionally, metamaterial structures are used to introduce desired phase shifts in microwave circuit applications. The Composite Right/Left Handed (CRLH) metamaterial structure has a unique feature of supporting an infinite wavelength at a nonzero frequency. This property of CRLH is leveraged to reduce the skew in the transmission of high speed clock signals over long nets.

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ABBREVIATIONS

VLSI	Very Large Scale Integration
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
MOS	Metal Oxide Semiconductor
DSM	Deep Submicron
RLGC	Resistance-Inductance-Conductance-Capacitance
CRLH	Composite Right/Left Hand
ZOR	Zero Order Resonance
MOR	Model Order Reduction
PCB	Printed Circuit Board
TL	Transmission Line
PLH	Pure Left Handed
PRH	Pure Right Handed
PCB	Printed Circuit Board

CHAPTER 1

Introduction and Preliminaries

1.1 Growth in the Integrated Circuit Technology

Invention of the transistor at Bell labs in 1947 and the formation of first Integrated Circuit (IC) chip by Jack S. Kilbey at Texas Instruments lab in 1958 opened the path for an unprecedented growth of the semiconductor technology. After its inception, productivity of the IC technology has increased more than a billion fold while performance has increased more than one hundred thousand fold over a span of fifty years (Bakir and Meindl, 2009). The tremendous growth in the semiconductor technology over the last five decades has immensely benefited every segment of human life.

Gordon Moore, one of the pioneers in the Silicon valley predicted the growth in the semiconductor industry in 1965 itself and formulated an empirical law stating that the number of components integrated into an IC will double every 24 months. This theory holds good even after 50 years of its inception and it is to continue in the foreseeable future (Iwai, 2009). Figure 1.1 shows the development of the process technology and how the die area has increased over a period of 40 years (from 1970 to 2010) (Chen, 2007). From the figure it can be seen that in the last 40 years, IC technology has scaled from 10 μm to 32 nm and the die area has grown approximately from 10 mm^2 to 500 mm^2. At the same time, the number of transistors integrated into an IC chip has grown roughly from 2300 to 2.6 billion components (Laker, 2011). Figure 1.2 shows the year of introduction of different processors along with the approximate number of components integrated in them during the period 1971 to 2011. International Technology Roadmap for Semiconductors (ITRS) association predicts Tera Scale Integration (TSI) (trillion transistors per chip) era in around 2022 (ITRS, 2009).

In order to sustain Moore's law, materials and technology used to fabricate the ICs have undergone revolutionary changes in the past five decades especially for the transistors and interconnect wires. In around 1960, circuits were constructed using Bipolar

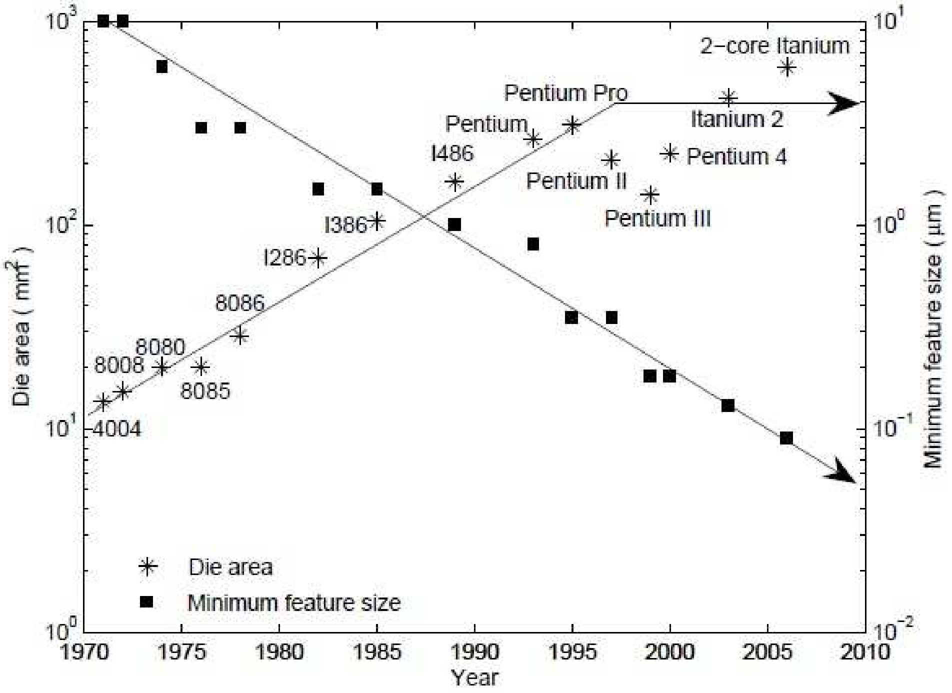


Figure 1.1: Development of technology node and die area (Chen, 2007)

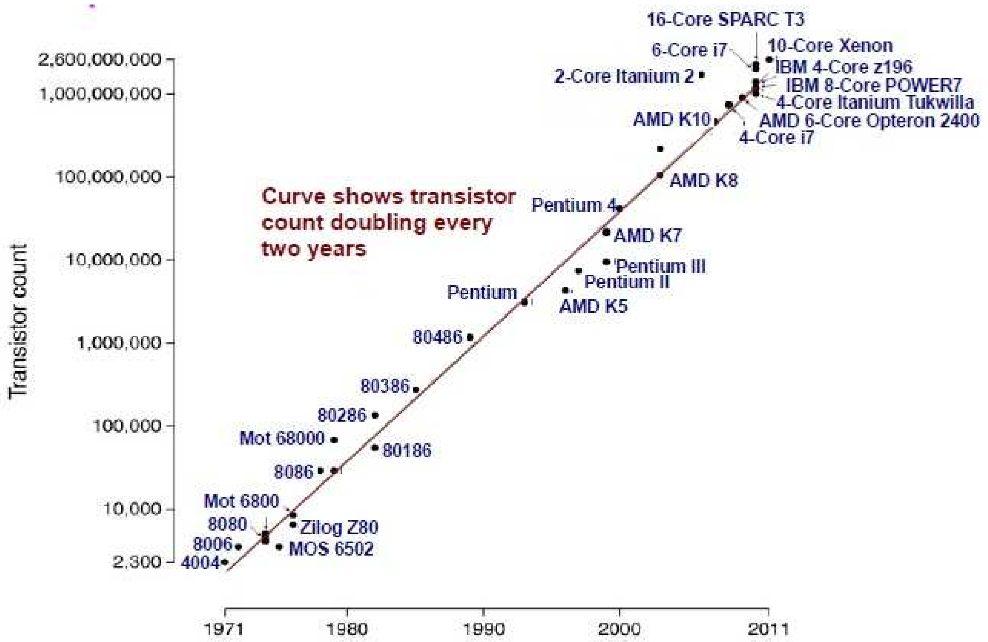


Figure 1.2: Approximate number of transistors integrated in different processor families (Laker, 2011)

Junction Transistors (BJT) and later switched to N-channel Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) in around 1970. Improvements in the performance and the power dissipation reduction in the circuit is brought out by Complementary Metal Oxide Semiconductor (CMOS) circuits in around 1980. With tremendous advancements and considerable refinements, CMOS has become a stable and dominant technology in the present day semiconductor industry (Bohr, 2007).

As the gate lengths of the MOS devices scaled below 100 *nm*, continued performance gains from scaling have slowed down (Thompson *et al.*, 1998). Some of the critical issues to be addressed at the transistor level in sub-100 *nm* in order to maintain the rate of progress of the microchip are gate tunneling current, sub-threshold leakage current and the demand for critical dimension tolerances.

Below 100 *nm* gate lengths, capacitive coupling effect between the source and drain increases. This increases Drain-Induced Barrier Lowering (DIBL) effect, reduces the threshold voltage and increases the gate leakage current. Technological improvements such as ultra-thin gate dielectrics, ultra-shallow source/drain junctions, halo implants etc. are used to overcome the above performance degrading effects in Deep Submicron (DSM) regime MOS transistors (Colinge, 2008).

Another fundamental limitation approaching in MOS devices due to scaling is the gate dielectric thickness. A thin gate dielectric increases capacitive coupling from the gate to the channel and thereby reduces the source/drain influence on the channel. Larger gate capacitance leads to increased ON-state drive current. However, gate dielectrics are already so thin that quantum mechanical direct tunneling through them results in significant gate leakage currents below $20\dot{A}$. The use of high-k gate dielectric materials provide a small effective oxide thickness to maintain adequate gate control needed for scaling while providing a large physical barrier to gate-oxide tunneling and thereby reducing gate leakage current (Colinge, 2008).

Shallow trenches are implanted at the source/drain junction to minimize dopant diffusion. The downside of this is, increase in the parasitic series resistance of the source and drain extension regions. In sub-100 *nm* gate length devices, a strong halo implant is generally used to suppress sub-surface leakage but this tends to increase the average channel doping in small gate length devices. However, high channel doping concentration reduces carrier mobility due to impurity scattering, resulting in increased transverse electric field, sub-threshold slope, band-to-band tunneling leakage, depletion and junction capacitances. All these factors together significantly degrades the device performance (Colinge, 2008).

In a continuous effort to increase the current drive capabilities and better control over short-channel effects in sub-100 *nm* gate lengths, traditionally used silicon dioxide and polysilicon gates for the fabrication of MOSFETs are replaced by high-k dielectrics and metal gates. Because of this, transistor switching speed is improved by 20% and gate leakage by more than tenfold (Kuhn, 2009). To enable future technology scaling, new device structures for the next-generation technologies have been proposed. Some of the most promising devices so far include Carbon Nanotube Field Effect Transistors (CNFETs), FinFETs, nanowire FETs, III/V compound-based devices, graphene nanoribbon devices, resonant tunneling diodes etc. (Colinge, 2008). Many of these devices have shown favorable device properties and characteristics to operate at sub-100 *nm* technology and require novel fabrication techniques. These nanoscale devices have significant potential to revolutionize the fabrication and integration of electronic systems and scale beyond the perceived scaling limitations of traditional CMOS.

One of the significant DSM regime problems created because of scaling is the rising interconnect delay. Increasing resistance of the wires is the main reason behind the rising interconnect delay in DSM regime ICs. Resistance is inversely proportional to the cross sectional area of the interconnects. To accommodate more functionalities and performances while fabricating an IC in successive technologies, large circuits with more components are used. These components are connected through interconnects and pitches of these wires dropping rapidly at about the same rate as the gate length. In order to control the sharp rise in the resistance, thickness of the interconnects are scaled at a slower rate, which results in taller and thinner wires. ITRS predicts that global interconnects Aspect Ratio (AR=height/width) will increase from 1.8 at 180 *nm* to 2.6 at 22 *nm* technology node (ITRS, 2009).

Instead of using high AR, the other approach to reduce the resistance of the lines is to use better conducting materials for the on-chip interconnects. This significant revolution occurred in the IC chip design when aluminum wires (existed from 1960 onwards) were replaced by copper wires in-around 1997. The resistivity of copper interconnects is approximately 30% smaller than that of aluminum interconnects (2.2 $\mu\Omega - cm$ vs. 3.2 $\mu\Omega - cm$). Another key advantage of using copper as the interconnect is that the resistance increases with the Electro Migration (EM) effect. Copper has a much lower susceptibility for the transportation to the metal ion from EM since it is a heavier metal. Usually, EM lifetime of copper is 100 times longer than aluminum wires at the same current density.

1.2 On-chip Interconnects in CMOS Technology

IC chips are made with different technologies and presently, CMOS is the most widely used technologies. In a CMOS technology, transistors are fabricated in a doped silicon substrate, usually with a gate of polysilicon on the top of oxide layer. In order to connect transistors, power, ground and clock lines, stack of metal layers are used as shown in figure 1.3 (ITRS, 2009). Vias are used to connect different metal layers and the space in between metal layers are filled with silicon oxide or some other dielectric material. Depending on the length, on-chip interconnects are classified into local, intermediate and global wires (Nurmi *et al.*, 2004). Local interconnects are very thin conductors used to connect gates and transistors within a functional block on a chip. These type of interconnects usually occupy the lower few layers in a multi-layered interconnect structure (figure 1.3). The dimensions of these interconnects scale down with the technology. Intermediate interconnects are those that are used to distribute clock/data signals within a functional block or between the adjacent blocks with typical lengths up to 2.5 *mm*. These type of wires occupy few layers above the local interconnects (figure 1.3). Global wires are the widest metal layers in a multi layer structure and occupy the top few layers. Typical lengths of these interconnects are greater than 2.5 *mm* and sometimes as long as half of the chip perimeter. Top metal layers are reserved

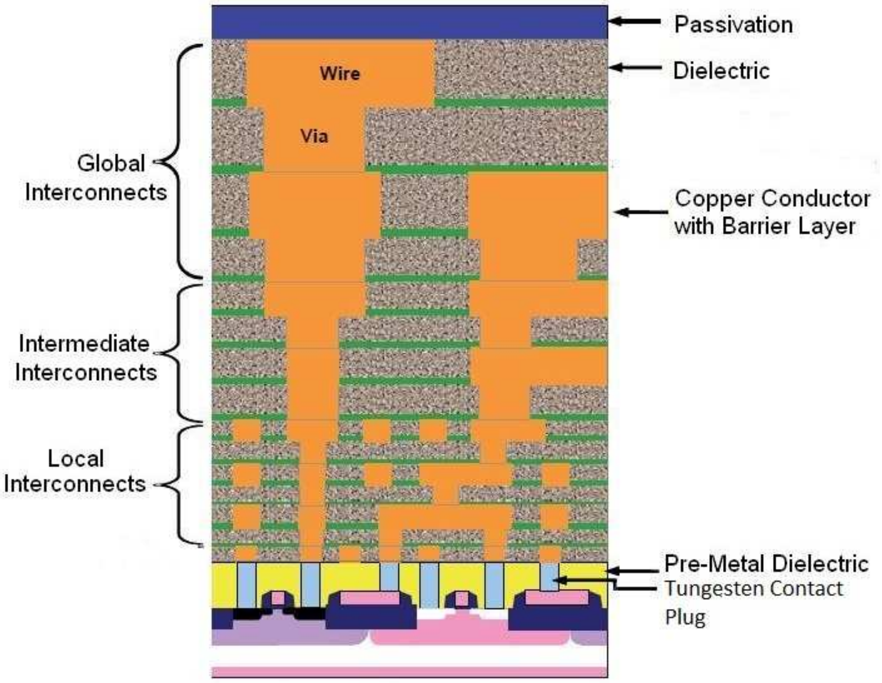


Figure 1.3: Cross sectional view on the stack of layers in an IC (ITRS, 2007)

for the routing of power/ground/clock signals. Dimensions of intermediate and global interconnects do not scale the same way as technology scaling.

1.2.1 Technology Scaling

The basic idea of scaling is to reduce the dimensions of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and associated interconnects to increase the performance and the component density per area. With the constant electric field scaling, the dimensions of the MOSFETs are scaled down by a factor of $\frac{1}{S}$ and the first order effects are given in table 1.1. This kind of scaling increases the device density by a factor of S^2 while decreasing gate delay and power dissipation by factors $\frac{1}{S}$ and $\frac{1}{S^2}$ respectively (Bakoglu, 1990). Thus, scaling of MOSFET dimensions increases the overall circuit performance.

Once considered to be electrically negligible, interconnects are becoming a major performance bottleneck in DSM regime high-performance ICs. This is because of the

Table 1.1: MOS scaling effects

Parameter	Scaling factor
Channel Length (L), Width (w), Gate oxide thickness (t_{ox}) and Voltage (V_{DD})	$1/S$
Current per device ($I_{DS} \propto \frac{w}{L}\frac{\varepsilon_{ox}}{t_{ox}}(V_{DD}-V_t)^2$)	$1/S$
Gate capacitance ($C_g \propto \varepsilon_{ox}\frac{wL}{t_{ox}}$)	$1/S$
Transistor ON resistance ($R_g \propto \frac{V_{DD}}{I_{DS}}$)	1
Gate delay (τ_g=$R_g \times C_g$)	$1/S$
Device area ($A_g = wL$)	$1/S^2$
Power dissipation ($P = I_{DS}V_{DD}$)	$1/S^2$

S: Scaling factor for device dimensions

increasing resistive, inductive and capacitive effects associated with the interconnects as chip size grows larger and interconnect geometries are scaled. As a result, these parameters significantly hamper the performance of high speed ICs in DSM regime.

Table 1.2 shows the ideal scaling (refers to the scaling of transistors and interconnects where all horizontal and vertical dimensions are reduced by the same factor) effects of local interconnect geometries (Bakoglu, 1990). Local interconnects length usually shrinks at the same rate of technology scaling. If it is assumed that all the local interconnect dimensions shrink by a factor of $\frac{1}{S}$, capacitance decreases by a factor of $\frac{1}{S}$ while resistance increases by S (table 1.2). Consequently, local interconnect delay remains unchanged.

Table 1.2: Ideal scaling of Local Interconnects

Parameter	Scaling factor
Local interconnect width (w), Substrate height (h), Spacing (s) and Thickness (t)	$1/S$
Local interconnect length (L_l)	$1/S$
Resistance ($R_l = \frac{\rho L_l}{wt}$)	S
Capacitance ($C_l = \frac{\varepsilon_{ox}w}{h} \times L_l$)	$1/S$
RC delay (τ)	1
Voltage drop (IR)	1
Current density (J)	S

S: Scaling factor for device dimensions

On the other hand, over the years, scaling has become a problem of growing importance in case of intermediate/global interconnects. The primary issue of scaling these interconnects is the problem associated with the growing system complexity. As the technology is scaled, length of the intermediate/global interconnects increases instead of shrinking. This is because, the chip area of each new technology generation keeps increasing to accommodate more functionalities and hence more components. This forces the intermediate/global interconnects to increase in length to connect all the devices.

Length of the intermediate/global interconnects is dependent on the chip area (A_c) and the length of the longest global interconnect in an IC chip is related to the chip area approximately by $\frac{\sqrt{A_c}}{2}$ (Nurmi *et al.*, 2004). Hence, during technology scaling, dimensions of these layers will not shrink in the same proportion as that of transistors gate length. Table 1.3 shows the ideal scaling effects of intermediate/global interconnects (Bakoglu, 1990). Scaling of the intermediate/global interconnects results in an increase in the delay in proportion to the wire length and the wire resistance.

Table 1.3: Ideal scaling of Intermediate/Global Interconnects

Parameter	Scaling factor
Intermediate/Global interconnect width (w), Substrate height (h), Spacing (s) and Thickness (t)	$1/S$
Intermediate/Global interconnect length (L_{gb})	S_c
Resistance ($R_{gb} = \frac{\rho L_{gb}}{wt}$)	$S^2 S_c$
Capacitance ($C_{gb} = \frac{\varepsilon_{ox} w}{h} \times L_{gb}$)	S_c
RC delay (τ)	$S^2 S_c^2$
Voltage drop (IR)	SS_c
Current density (J)	S

S_c: Scaling factor for chip size

In summary, technology scaling decreases the gate delay (transistor delay) and wire delay of the local interconnects while delay in the intermediate/global interconnect increases. Advanced scaling techniques (such as weak scaling of wire thickness and usage of low dielectric constant insulator material) improves the situation somewhat, so that wire delays almost track the improvement in gate delays. However, intermediate/global interconnect delays become much worse than gate delays in every successive technology nodes below 0.25 μm as can be seen from figure 1.4. Further, as the interconnect delay increases, it results in more power consumption, signal attenuation etc. (Ismail *et al.*, 1999). Thus the intermediate/global interconnect delay, rather than the gate delay, becomes a limiting factor in determining the overall circuit performance in the present day Very Large Scale Integration (VLSI) chips.

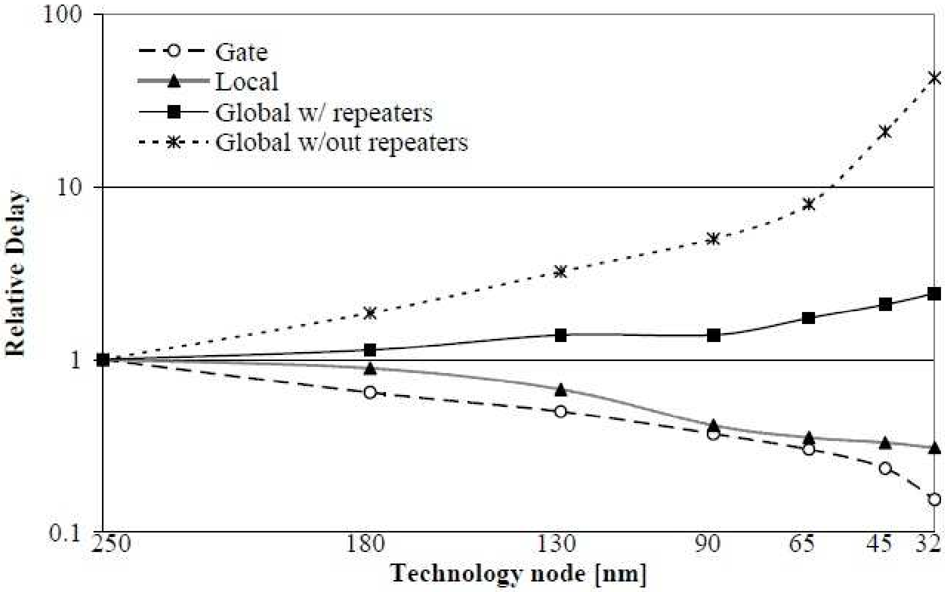


Figure 1.4: On-chip interconnect delay across different technology nodes (reproduced from (ITRS, 2007))

1.2.2 ITRS Predictions

According to ITRS predictions on the future trend in interconnect dimensions, delay, technology nodes etc. given in table 1.4 (ITRS, 2007). On-chip total interconnect length increases linearly with technology and will approach 9000 m/cm^2 by 2022. This supports the assumption of long interconnects occupying large die area in future technologies (approximately 450 mm^2 by 2022). It is also predicted that the delay of intermediate and global copper interconnects will increase quadratically with technology and may reach to 47 *ns* and 11.5 *ns* respectively for 1 *mm* long interconnect by the end of 2022. When the interconnect geometries are scaled, width of the interconnects decreases and RC time constant increases due to increased resistance and decreased cross section. This trend shows that scaled intermediate/global interconnect exhibit increase in the latency.

Table 1.4: ITRS 2007 prediction on scaling trends

Parameter	2007	2010	2013	2016	2019	2022
Technology Node (nm)	65	45	32	22	16	11
Number of metal levels	11	12	13	13	14	15
Total interconnect length (m/cm^2)	1439	2222	3125	4545	6250	9091
Intermediate wiring pitch(nm)	136	90	64	44	32	23
Aspect Ratio (AR) of intermediate interconnects	1.8	1.8	1.9	2.0	2.0	2.1
Intermediate interconnects RC delay (ps)	741	1892	4044	9127	19700	46741
Global interconnect wire pitch (nm)	210	135	96	66	48	33
AR of global interconnects	2.3	2.4	2.5	2.6	2.8	2.9
Global interconnects RC delay(ps)	227	542	1129	2476	4978	11437
Effective dielectric constant (k)	2.9-3.3	2.6-2.9	2.4-2.8	2.1-2.5	2.0-2.3	1.7-2.0
Copper resistivity ($\mu\Omega - cm$)	3.51	4.08	4.83	6.01	7.34	9.84
Wafer diameter (mm)	300	300	300	450	450	450

As per the ITRS roadmap (ITRS, 2009), presently feature sizes of the devices are scaling down roughly at a rate of 0.7 in every two years. This results in the doubling of gate density, reduction of gate delay by 30% and reduction of energy per switching by 65%. Thus, scaling down of transistor dimensions lead to improvements in both cost and performance. However, with scaling, the interconnects become taller and narrower resulting in the increase of resistance per unit length at the rate of 104% per year (Nigussie, 2011).

The lengths of the local interconnects scale down the same way as the transistor gate lengths whereas intermediate/global interconnects tend to track the chip dimensions. In general, die area should decrease by 50% in successive technology generations but new designs integrate more transistors and functionalities per chip, resulting in a need for more die area. Over the years, die area increases roughly 13% per year and consequently, the total interconnect length increases at a rate of 6% per year resulting in an overall increase of interconnect delay by approximately 120% (Nigussie, 2011). More delay implies increased power consumption, signal attenuation, ringing effects etc. Hence, intermediate/global interconnects play a major role in determining the performance of the present day ICs. This demands the circuit designers to put higher efforts in the design and optimization of long interconnects.

1.2.3 Interconnect Characteristics

Since long interconnects become a dominant factor in deciding the performance of high speed ICs, focus of the circuit design process has shifted from logic optimization to interconnect optimization, viz., optimization of interconnect delay, power dissipation, crosstalk noise, bandwidth, physical area, transmission line effects, parasitic modeling etc. These issues are briefly discussed next.

1.2.3.1 Interconnect Delay

Delay is the primary performance metric for interconnects since the circuit speed is limited by the signal propagation time over wires. Interconnect delay is defined as the difference between the time during which the logic transitions at the source and the sink cross 50% of their amplitude values. Input and output waveforms are characterized by the rise time, t_r and the fall time, t_f and are defined as the time taken to reach from 10% to 90% of the respective voltage transitions.

Just as the technology advances, the delay models also become more complex and sophisticated. In early VLSI designs, interconnects were modeled as lumped capacitive loads for gates and the wire resistance was ignored. With scaling, the interconnect resistance started affecting the signal characteristics and accordingly, delay models had to be changed to include wire resistance. This gave rise to lumped RC models. Later, more accurate distributed RC models came into effect (Nurmi *et al.*, 2004). One of the most popular RC delay estimation models for the branched and non-branched RC network is Elmore time constant (Elmore, 1948).

As the technology is scaled below 0.25 μm, signaling frequencies exceed a few

GHz and their rise times getting limited to a few pico-seconds, interconnects need to be treated as transmission lines. In such cases, distributed RC models are inadequate to accurately model delay because RC models cannot model higher-order systems. It is found that second or higher order RLC models of the interconnect provide significant improvements over the accuracy of a first-order RC delay model. A detailed second order RLC delay model for a nonlinear driver and a single transmission line is presented in (Boese *et al.*, 1992). Closed-form solutions for the 50% delay, rise time, overshoots and settling time of signals in a second-order RLC tree are presented in (Ismail *et al.*, 2000) Apart form this, various types of delay estimation models based on different interconnect equivalent models are derived as evident from the previously published work (Achar and Nakhla, 2001).

1.2.3.2 Power Dissipation

Due to higher clock frequencies and longer interconnect lengths, overall power dissipation in an IC increases significantly with technology scaling. On-chip power dissipation in current general purpose microprocessors vary in the range 10-100's of watts. Figure 1.5 shows the components of dynamic power due to different capacitive sources in a microprocessor (Chen, 2007). Form the figure, it can be seen that the dynamic power dissipation due to interconnect capacitance alone is greater than 50% of the total dynamic power. If repeaters and pipeline registers are inserted in the interconnects, these circuits will introduce additional dynamic, leakage and short-circuit power. Higher power dissipation increases the packaging cost due to heating problems and shortens the battery life in portable applications. Therefore, power dissipation is another important criterion that should be considered in the interconnect design.

1.2.3.3 Crosstalk Noise

In a multi-layered IC, interconnects are closely placed and with scaling, coupling capacitances among interconnects dominate over the ground capacitances. Further, at GHz frequencies, inductive coupling and the associated coupling noise become signif-

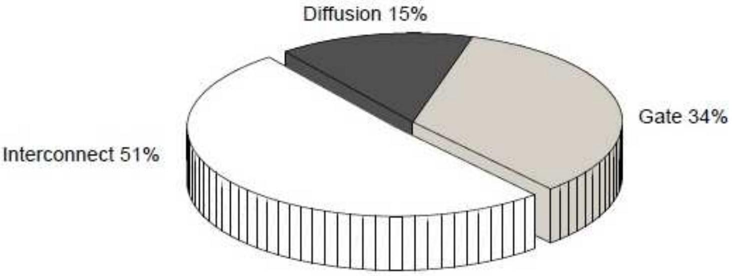


Figure 1.5: Dynamic power dissipation due to different capacitive sources in a microprocessor (Chen, 2007)

icant. Coupling affects the interconnect performance in two ways, viz., fluctuation in the output voltage level and delay uncertainty, as shown in figure 1.6 (Chen, 2007). If the crosstalk noise level is greater than certain threshold limit, it causes malfunctioning of the circuit. In addition to the coupling effects, delay uncertainty is caused by factors such as process variations, temperature variations, power/ground noise etc. If the delay uncertainty exceeds some threshold level, it will cause setup and/or hold time violations and thereby further degrading the system performance.

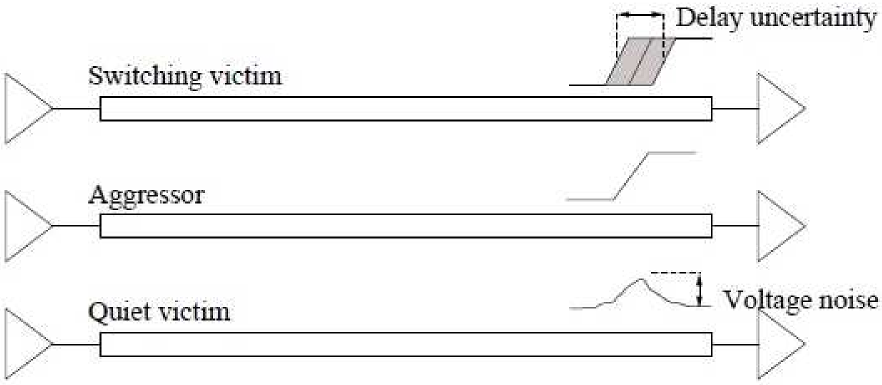


Figure 1.6: Delay uncertainty and crosstalk noise in closely placed interconnects (Chen, 2007)

1.2.3.4 Bandwidth (B)

For on-chip applications, bandwidth (the number of bits transmitted per second) is a measure of data transmitting capacity of the interconnect. A higher bandwidth reduces the total time required to transmit a certain amount of data, thereby increasing the system performance. A bit period can be divided into two parts namely transition time and steady state time. During the steady state time, data is latched at the receiving register. If it is assumed that the steady state part occupies at least half of the bit period, the maximum bandwidth is related to the rise/fall time (t_r) as (Chen, 2007)

$$B = \frac{1}{2t_r} \tag{1.1}$$

1.2.3.5 Physical Area

Despite technology scaling, the die size remains more or less constant or may increase owing to the integration of additional features (ITRS, 2009). In the present day ICs, the total interconnect length is significantly high (several hundreds of meters per centimeter area) and it is increasing with technology scaling. Also, the number of metal layers are increased to provide sufficient metal resources for routing. Increased functionality, longer interconnect lengths and increased number of metal layers - all add up to the fabrication cost and power dissipation. Therefore, die area is another key metric that need to be considered during the interconnect design process.

1.2.3.6 Transmission Line Effects

When the interconnects are longer than $\frac{1}{10}$th of the wavelength of the signal transmitted, neglecting the wave nature of the propagated signals results in error in the analysis. The wave nature of the signals show variations in the signal amplitude along the interconnect length due to the phase differences. Such lines are considered electrically long and need to be modeled as transmission lines (Nurmi *et al.*, 2004). When the interconnects act as transmission lines, signals get reflected when there are impedance mismatches or discontinuities in the line. The reflection coefficient is given as

$$\Gamma = \frac{V_r}{V_i} = \frac{Z_d - Z_o}{Z_d + Z_o} \tag{1.2}$$

where Z_o is the characteristic impedance of the interconnect and Z_d is the impedance of the discontinuity. Few examples that give rises to basic discontinuities are series inductance, shunt capacitance, capacitive loads, unmatched terminations etc., which arise from physical changes in the signal paths due to vias, wire bends, stubs, wire crossovers, bonding wires, package pins, connectors, non-ideal receivers etc.

1.2.4 Interconnect Parameters

On-chip interconnect structures are usually composed of metal lines with rectangular cross sections (Manhattan style layout) of layers. This architecture reduces the complexity of modeling, routing algorithms and at the same time greatly simplifies the manufacturing process. A cross sectional view of the top and intermediate layer interconnects are shown in figure 1.7 along with the geometric parameter definitions. Symbols *w*, *s*, *t* and *h* refer to the interconnect width, spacing between the lines, thickness and dielectric height respectively. The interconnect parasitics are extracted from the geometry of the interconnect structures and are illustrated in the following subsections.

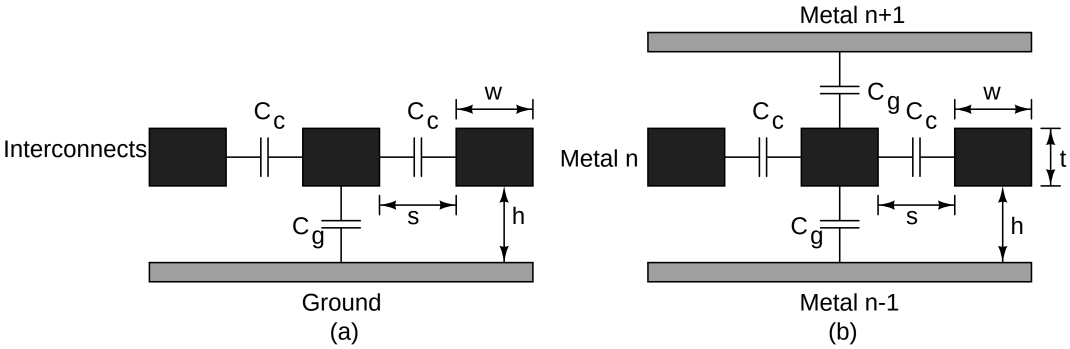


Figure 1.7: Cross sectional view of the (a)Top layer interconnects and (b) Intermediate layer interconnects (Wong *et al.*, 2005)

1.2.4.1 Resistance (R)

For a uniform interconnect of width *w* and thickness *t* (figure 1.7), its DC resistance is calculated as

$$R = \frac{\rho l}{wt} \tag{1.3}$$

where ρ is the resistivity of the interconnect material (2.2 $\mu\Omega$-cm for copper and 3.3 $\mu\Omega$-cm for aluminum). In addition to this, vias, which connect multiple layers vertically, contribute to path resistance as well.

Resistance with Skin Effect

At high frequencies, the current density inside a conductor is not uniform, but drops away exponentially with depth into the conductor. A cut-off frequency where this phenomenon begins can be identified and an empirical approximation for this value is given by (Dally and Poulton, 1998)

$$f_c = \frac{\rho}{\pi\mu\delta_c^2} \tag{1.4}$$

where μ refers to the dielectric permeability, and δ_c to the skin depth as given in equation (1.5). The last equation is an approximation given in (Zheng, 2001).

$$\delta_c = 1.5tw(h+w) \tag{1.5}$$

Below f_c, the current is assumed to be spread uniformly across the entire cross-sectional area of the conductor, resulting in the DC resistance given in equation (1.3), while above it, the resistance increases with the square of the frequency. Hence the frequency dependent resistance R_{HF} can be conveniently expressed as given in equation (1.6).

$$R_{HF} = R\left(\frac{f}{f_c}\right)^{1/2} \tag{1.6}$$

1.2.4.2 Inductance (L)

Inductive effects become significant in the nanometer regime particularly for intermediate and global interconnects. The fundamental definition of L is

$$L = \frac{\oint_A B ds}{I} \tag{1.7}$$

where I is the current, B the magnetic field induced from I and s is the integration loop. If s is same as I, L is termed as self-inductance,whereas if s follows a different conducting path, equation (1.7) defines mutual inductance (M). This indicates that the inductance calculations follow a loop property and thus the determination of inductive behavior should consider the entire current loop. However, in modern interconnect structures, there are no DC paths to form well defined loops. As a result, return current usually spreads over a long range, which complicates the analysis. Consequently, the extraction analysis should include all neighboring lines that are possibly involved in the current loops (Wong *et al.*, 2005).

Because of the uncertainty of the return current path, it is difficult to calculate loop inductance in realistic designs. This difficulty is overcome by the concept of partial inductance, in which the induced current is assumed to return at infinity and avoids the need to define the return loop. Closed-form solutions to calculate the self inductance and mutual inductance for rectangular cross-sectional interconnects are derived and simplified to the following relationships when $l >> w$, t and d ((Qi *et al.*, 2000), (Wong *et al.*, 2005)) .

$$L = \frac{\mu}{2\pi}\left[l\ln\left(\frac{2l}{w+t}\right)+\frac{l}{2}+0.2235(w+t)\right] \tag{1.8}$$

$$M = \frac{\mu}{2\pi}\left[l\ln\left(\frac{2l}{d}\right)-1+d\right] \tag{1.9}$$

where w, t and l are the width, thickness and length of the segment respectively and d is the center-to-center distance between the interconnects.

1.2.4.3 Capacitance (C)

Capacitance is a measure of coupling between the interconnects through electric fields. If the layers above and below a line are routed densely, they can be approximated as a ground plane, leading to two-dimensional models as shown in figure 1.7. Depending on whether or not the coupling interconnect is grounded, it is classified mainly into two types, namely, metal-to-ground capacitance (C_g) and metal-to-metal capacitance (CC). Capacitive coupling is a short-range effect and when there are multiple lines on the same layer, capacitive coupling decays rapidly with the increase in neighboring orders.

To achieve simplicity in modeling while maintaining sufficient analysis accuracy, only the nearest CC values are considered in extraction and performance analyses while the higher-order CC values are neglected as a first approximation. A comprehensive study of coupling capacitance between different layers of interconnects under varied width and scaling is presented in (He, 1999) and a parametric dependence of interconnect capacitance is presented in (Goel, 2007). If the layers above and below a line are routed densely, they are approximated as ground planes and lead to two-dimensional models. Under these conditions, C_g and CC becomes scalable function of cross-sectional dimensions. Analytical models for C_g and CC of the intermediate/global interconnects are given as ((Wong *et al.*, 2000), (Wong *et al.*, 2005))

$$C_g = \varepsilon \left[\frac{w}{h} + 2.217 \left(\frac{s}{s + 0.702h} \right)^{3.193} + 1.171 \left(\frac{s}{s + 1.510h} \right)^{0.7642} \left(\frac{t}{t + 4.532h} \right)^{0.1204} \right] \tag{1.10}$$

$$\begin{aligned} CC \quad = \quad & \varepsilon[1.144 \frac{t}{s} \left(\frac{h}{h + 2.059s} \right)^{0.0944} + 0.7428 \left(\frac{w}{w + 1.592s} \right)^{1.144} \\ & + 1.158 \left(\frac{w}{w + 1.874s} \right)^{0.1612} \left(\frac{h}{h + 0.9801s} \right)^{1.179}] \end{aligned} \tag{1.11}$$

$$C = C_g + 2CC \tag{1.12}$$

where ε is the dielectric constant and dimension variables are as defined in figure 1.7. These models are generated from physical considerations and the coefficient values are fitted from field solver results. After two-dimensional values of C_g and CC per unit length are obtained, the total capacitance is calculated by multiplying them by the length of the line.

1.2.4.4 Conductance (G)

Since the signals propagate in GHz regime, the loss in the dielectric layer needs to be considered. The conductance is estimated by a parallel plate structure and represented as (Jun-De JIN *et al.*, 2008)

$$G = \varepsilon \omega \frac{w}{t} \tag{1.13}$$

where ω is the angular frequency. From equation (1.13), it is expected that the conductance increases in proportion to the increase in the operational frequency.

1.2.5 Interconnect Effects in DSM Regime

In VLSI technology generations of 0.25 μm and below, intermediate/global interconnect effects are becoming dominant factors in determining the chip performance (figure 1.4). Some of the predominant interconnect effects in DSM regime are listed below (Nurmi *et al.*, 2004).

- As chip speed increases, inductance effect increases which will cause ringing effects at signal rise or fall edge.
- The number of metal layers in current state-of-the-art technologies is nine and is expected to increase to 13 in 22 *nm* technology node. The additional metal layers will further increase the dynamic power dissipation by the interconnects due to the increased parasitics associated with the interconnect.
- Thinner and higher aspect ratio of the interconnects increases both the capacitive and inductive voltage coupling effects. This raises the amount of coupled crosstalk noise voltage to the neighboring interconnects.
- Increase in the length of intermediate/global interconnects results in linear or quadratic increase in the latency.
- In GHz frequency regime, interconnects behave as transmission lines. Because of this, transmission line effects such as signal reflections arise at the impedance discontinuity junctions.
- As the supply voltage is scaled, noise margins of the circuit decreases and make the circuit more sensitive to the injected noise.

Interconnects are one of the main sources of noise, such as coupling noise, IR and $L\frac{di}{dt}$ drops across power/ground lines, jitter/skew in the clock distribution network etc. The design of on-chip interconnects therefore has become an essential performance metric in high speed ICs. In this work, the focus is in providing solutions to deteriorating interconnect effects on data/clock signals in DSM regime.

1.3 Challenges and Motivation for Modeling, Analysis and Optimization of Interconnects in GHz Regime

When the transistor and interconnect dimensions are in micro-meters, interconnect effects such as delay and crosstalk noise are less of a problem and hence circuit designers could safely ignore these effects or at-most use approximate lumped RC models for analyses. As the geometries of the scaled transistors and interconnects entered nanometer dimensions, interconnects begin to affect the circuit performance and the designers are compelled to consider their effects. Hence advance knowledge on the accurate interconnect metrics (like delay, rise time, overshoot and undershoot time, cutoff frequency etc.) is important for the designer to chalk out plans to reduce these effects to a maximum extent. These parameters are estimated from the mathematical models and are derived by replacing the interconnects with suitable equivalent circuits.

Over the years, interconnects are represented by several equivalent circuit models like lumped C, lumped RC, distributed RLC etc. In these models, the interconnect metrics are estimated from an approximation of transfer function coefficients. Different models for estimating interconnect metrics are available for single line interconnects while very few are reported employing RLGC models for coupled interconnects. Further, these models can not be generalized and extended for analyzing multi-coupled interconnect lines.

Interconnects with Manhattan geometry have general shapes such as **L**, **U**$(\sqcup \text{ o}r \sqsubset)$, **Z**$(\urcorner\!\llcorner)$ and **T** $(\top)$. Up-until now, to our best knowledge, models to estimate the interconnect metrics for these shapes are not available. Also, well-defined models for the estimation of crosstalk noise in the victim lines of the multi-coupled interconnects (multiple number of coupled interconnect lines) are not presented in previous literatures. In this work, these problems have been addressed by modeling different interconnect shapes using state space approach.

To reduce the intermediate/global interconnect delay, various techniques have been developed starting from repeater insertion to low voltage signaling. Exploiting interconnect capacitance was another approach employed to reduce the delay. Further, demand for low power techniques brought in the concept of quasi-resonant interconnects. The idea is to make a resonating interconnect by inserting an inductor of appropriate value along the interconnect so as to make the interconnect capacitance to resonate around the fundamental frequency of the signal. As the circuit (”interconnect”) is under resonance, the energy resonates between electric and magnetic fields rather than dissipating it as heat. Main drawbacks of this scheme are that the large area overhead for the on-chip passive inductors and large number of parasitics associated with the structure.

Unlike local interconnects, intermediate and global interconnects have a greater reach across the IC and distribute signals to different parts of the circuits that are geometrically apart. These wires invariably use vias to deliver the signals to the local interconnects and to the devices. At high frequencies, the impedance discontinuity at the junction of on-chip intermediate/global interconnect and via results in signal reflections and contributes to the loss of signal. Different techniques are reported in the literature to reduce the signal reflections in multi-layered interconnect structures. In all these papers, the reduction in signal reflection is achieved by modifying the via structure and it is mostly aimed at Printed Circuit Boards (PCBs). Further, in these cases the structure (geometry) of the vias once fabricated remains fixed and modification of via geometry is not feasible to suit newer frequencies of operation.

In high speed digital ICs, usually clock signals are transmitted using a tree structure (e.g., H-tree, binary tree, fanout balanced tree etc.). In DSM regime, clock signals also suffer from signal degradation effects such as increased propagation delay, skew, jitter etc. These effects become more acute with the increase in frequency of operation and limit the maximum speed and efficiency of the IC chips. Composite Right/Left Handed (CRLH) structures find their use as delay lines in signal processing applications, microwave, radar and phased array systems. The CRLH structure has a unique feature of supporting an infinite wavelength at a finite non-zero frequency. This property of CRLH structure can be used to reduce clock skew in high speed applications.

The challenges posed by interconnects with technology scaling are numerous and those listed above are only representative in nature. Interconnects are thus becoming serious performance bottlenecks in the present day high-speed IC design and there is a pressing need to address these issues at all levels of design hierarchy.

1.4 Major Research Contributions

Technology scaling improves the performance of the transistors while degrading the intermediate/global interconnect performance (see figure 1.4). In this thesis, circuit level methods to improve the performance of the intermediate/global interconnects have been suggested. To deal the problem at hand, in advance the designers should be able to estimate proper interconnect metric values from the interconnect equivalent models. The first step in this direction is to use appropriate interconnect equivalent models. With the IC operation frequencies entering into GHz regime, interconnects tend to behave as transmission lines. To include the transmission line effects in the model, interconnects are modeled as a distributed RLGC network.

Major contributions of this thesis are summarized below.

- Using State Space approach, generalized state space matrices are derived for Single, Coupled, **L** and **T** type interconnects by considering the mutual inductive and coupling capacitive effects between the adjacent lines and layers. The derived models are general and modular in nature. Using these models, interconnect metrics for any length and shape can be estimated. Further, these models can be used to estimate coupled noise voltages in the victim lines in a multi-coupled interconnect environment.

- It is shown that the use of active inductor in place of passive inductor in the Resonant Interconnect Network (RIN) helps to reduce delay, area and crosstalk in the interconnect network. Mathematical model for the RIN section employing active inductor is derived using state space approach. The results are promising and closely match with the SPICE simulations. Monte Carlo simulations show that the change in the interconnect delay behavior for the process and mismatch variations in the active inductor circuit as well as interconnect parameters are insignificant. Further, the silicon area required to fabricate active inductor is found to be orders of magnitude smaller than that required for passive inductor and that the far end coupled noise also reduces by more than 50%.

- At GHz frequencies, impedance mismatch at on-chip via-interconnect junction pose problems for signal integrity. At these frequencies, on-chip vias being predominantly inductive and resistive in nature, reduction of via-induced signal reflection can be addressed by incorporating a capacitive load at the interconnect-via junction. The capacitance value required for impedance matching can be derived from the knowledge of interconnect and via parameters. Further, if the operating frequency need to be altered, capacitance tuning can be achieved easily and without requiring any modifications to the interconnect geometry.

- The reduction of clock skew is addressed by augmenting a CRLH metamaterial structure in the clock network. The geometry of the metameterial structure is chosen such that it resonates with a Zeroth Order Resonance (ZOR) frequency close to the desired clock frequency. At resonance, the delay introduced by the interconnect is close to zero and the clock edge arrives at the destination almost with zero skew.

1.5 Thesis Organization

The contents of the thesis and its organization is as follows.

- Chapter 2 presents a brief introduction to the previously used different interconnect models and interconnect metrics estimation models.This is followed by representing the interconnects using distributed RLGC network and modeling different interconnect shapes using State Space approach.

- Chapter 3 presents crosstalk estimation model of the victim line of the two-coupled interconnects using State Space approach and extension to five-coupled interconnect system. Also, reducing the order of the distributed RLGC network using Moment Matching technique is discussed in this chapter.

- Chapter 4 addresses the issue of reducing the interconnect delay in resonant interconnect network using on-chip active inductors. Time domain simulations and analysis on the crosstalk noise voltage in the coupled resonant interconnect lines employing active inductors are also presented in this chapter.

- Chapter 5 presents a brief description of interconnect behavior in GHz frequencies, problems associated in this regime and the previous methods used to overcome the problems are discussed in the introduction. In this chapter, a simple method to minimize the impedance mismatch between interconnect-via junction is presented.

- Chapter 6 presents a brief description of CRLH metamaterial theory followed by a technique employing a CRLH structure in a long interconnect line to reduce the interconnect delay in high speed clock networks.
- Chapter 7 presents conclusions and scope for future work.

CHAPTER 2

RLGC Based Interconnect Modeling using State Space Approach

2.1 Introduction

Current trends of VLSI technology scaling and increase of clock frequencies is predicted to continue in foreseeable future. Shrinking feature sizes mean decreased transistor dimensions and interconnect geometries and thereby making it possible to place more components and pack more number of interconnect levels in successive technology generation ICs. Scaling also makes the interconnects thinner and taller, resulting in reduced fringing capacitance and capacitance-to-ground effects. However, the wire resistances and the coupling capacitances increase at a faster rate, diminishing the gains of reduced area and spacing between the closely placed interconnects. Die size remains relatively constant or increases marginally in successive technology generations as more and more functionalities are integrated into a single chip. Since the lengths of the intermediate and global interconnects depend on the die area, they introduce longer signal delays vis-a-vis gate delays. Thus, in today's DSM regime, the role of on-chip intermediate/global interconnects becomes increasingly dominant in determining the overall circuit performance.

Ability to put billions of transistors on a millimeter die area has increased the computational complexity of delay models used in a design flow. According to ITRS predictions, by the end of year 2022, the number of metal levels, total interconnect lengths, intermediate/global interconnect delay in a 1 mm copper wire and capacitance per unit length (intermediate as well as global interconnect) would respectively increase to 15, 9000 m/cm^2, 10.4/4 ns and 1.4 pF/cm (ITRS, 2009). Hence an accurate interconnect modeling is important in DSM chip designs to ensure better yield early in the design cycle. To this end, it is necessary to accurately estimate the effects of on-chip interconnect parasitics on signal properties such as delay, rise/fall time, overshoot time, cut-off frequency etc. during the design and integration of VLSI circuit blocks. These parameters are estimated from the interconnect equivalent models.

2.2 Interconnect Modeling

The ideal approximation of a wire assumes that it can be treated as an equipotential region without any loss. A real wire however presents a load to the signal driver, requires non-zero time for the signal to propagate across it (sometimes requiring multiple reflections), and consumes power. At frequencies where the circuit dimensions become comparable to signal wavelengths, the parasitics of the interconnect begin to show loading effects on the signal driver circuits, introducing signal delays, signal degradation and power dissipation. Over the years, different types of models are developed to analyze interconnect non-idealities. Models differ depending on the dimensions of the interconnects and rise (and fall) time of the signals with which they are gated. The rest of the section gives a brief introduction to field solvers, and then presents some of the commonly used interconnect equivalent networks in modeling.

2.2.1 Field Solvers

The accurate extraction of parasitics requires solving Maxwell's equations in 3 dimensions, which is accomplished by tools known as field solvers. Using a 3D field solver is very expensive computationally, and impossible over an entire chip, or even large subcircuits. A second class of tools that consider strips or slots with uniform cross-sections and sacrifice accuracy for run time reduction, are known as 2D field solvers. A third class that falls in between these two are named (predictably) 2.5D field solvers. They allow arbitrary metal patterns in one or more planes, and discretized only the metal in each plane. Usually using even a 2D field solver is justified only for the most critical portions of the chip.

A field solver uses numerical techniques to solve for the fields in the regions of interest, from which the required frequency dependent parameters such as capacitance or inductance are extracted. These numerical techniques have been classified under various names depending on their approach (Hubing, 1991; Pamunuwa, 2003).

2.2.1.1 Finite Element Method (FEM)

A Finite-Element Analysis (FEA) discretizes a continuous domain into a number of small homogeneous elements so that the field variation within the element can be approximated by simple models. These elements are connected to each other through nodal points. Most FEMs use variational techniques to obtain the field solution at each node. That is, some expression known to be stationery about the true solution is minimized or maximized at each node, that together with the boundary conditions result in a set of algebraic equations, the solutions to which result in the parameter of interest at each node.

2.2.1.2 Moment Method

The method of moments (MoM) refers to an FEA that uses the Method of Weighted Residuals (MWR) to solve a set of differential equations at each node. The MWR reaches a solution in a leap-frog manner by substituting an approximate solution into the equations and then summing the weighted residual iteratively until the solution converges. Hence it is an integral solution method.

2.2.1.3 Boundary Element Method (BEM)

BEM is essentially a subset of the method of moments. It is a moment-method technique whose expansion and weighting functions are defined only on a boundary surface. It is derived through the discretization of an integral equation that is mathematically equivalent to the partial differential equation that governs the solution in a domain. Most moment methods utilize a BEM technique in a general purpose solver.

2.2.1.4 Finite Difference Time Domain (FDTD) Method

In the FDTD method, Maxwell's (differential form) equations are simply modified to central-difference equations, discretized, and solved iteratively. Maxwell's curl equations are:

$$\nabla \times H = J + \varepsilon \frac{\partial E}{\partial t} \tag{2.1}$$

$$\nabla \times E = -\mu \frac{\partial H}{\partial t} \tag{2.2}$$

From an examination of equation (2.1) and equation (2.2) it can be seen that the time derivative of the E-field is dependent on the curl of the H-field. This can be simplified to state that the temporal change in the E-field (the time derivative) is dependent on the spatial change in the H-field (the curl). The result is the basic FDTD equation that the new value of the E-field is dependent on the old value of the E-field (hence the difference in time) and the difference in the old value of the H-field on either side of the point in consideration in space. The H-field is found in the same manner.

2.2.1.5 Finite Difference Frequency Domain (FDFD) Method

Similar to FDTD techniques, FDFD results from a finite difference approximation of Maxwell's curl equations. However now the time harmonic versions of the equations are employed:

$$\nabla \times H = (\sigma + j\omega\varepsilon) E \tag{2.3}$$

$$\nabla \times E = -j\omega\mu H \tag{2.4}$$

Since there is no time stepping, uniformity of mesh spacing is not required. Hence optimal FDFD meshes resemble optimal finite-element meshes.

2.2.1.6 Transmission Line Matrix (TLM) Method

In the TLM method, analysis is performed in the time domain and the entire region of the analysis is gridded similar to FDTD. Instead of interleaving the E-field and H-field grids however, a single grid is established and the nodes of this grid are interconnected by virtual transmission lines. Excitations at the source nodes propagate to adjacent nodes through these transmission lines at each time step.

2.2.1.7 Partial-Element Equivalent Circuit (PEEC) Method

Methods involving PEEC models are very popular because they allow a quasi-static analysis with equivalent elements of resistors, capacitors and inductors. From Maxwell's differential equations, a single integro-differential equation that describes the E-field can be constructed:

$$E(r,t) = \frac{J(r,t)}{\sigma} + \frac{\partial}{\partial t}A(r,t) + \nabla\Phi(r,t) \tag{2.5}$$

Each term of equation (2.5) can be used to define an equivalent circuit element for each metal segment in the grid, with the first corresponding to the resistive term, the second to the inductive term and the third to the capacitive term. Subsequently KVL and KCL are used to solve the resulting circuits using a circuit simulator such as SPICE.

Several techniques other than the ones described above have been developed, and a good overview can be found in (Hubing, 1991). For the most part, the use of field solvers is restricted to critical portions of the chip due to the complexity of the numerical techniques and the consequent high run time. Alternative approaches to model resistive, capacitive and inductive parasitics that are cheaper, though necessarily less accurate are examined. These are important in their own right, as they provide an intuitive understanding of the variation in performance with geometry, and are perfectly adequate for a large number of cases.

2.2.2 Interconnect Equivalent Models

2.2.2.1 Lumped Capacitance Modeling

When wider geometries of metal lines are used, the parasitics (figure 2.1.a) of the interconnect are found to be predominantly capacitive in nature. While modeling such an interconnect at low frequencies, the parasitics (C_{int}) are either completely neglected or replaced by an equivalent lumped capacitance (C_{lump}) as shown in figure 2.1.b. In this figure the driver circuit is replaced with a voltage source (V_{in}) in series with a resistance (R_d) (Rabaey *et al.*, 2002).

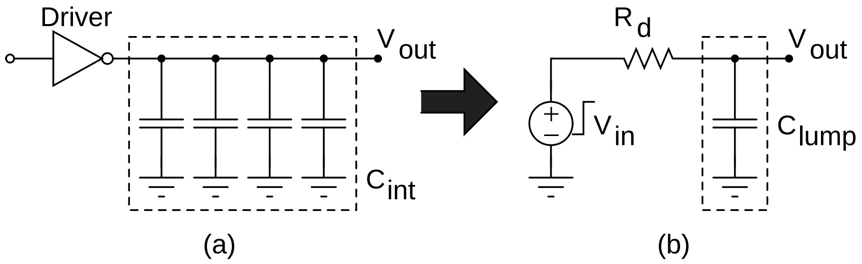


Figure 2.1: Lumped capacitance equivalent model

In these type of models, interconnects represent an equipotential region and will not introduce any delay. The parameter that impacts the performance of the circuit is the loading effect of the capacitor on the driving gate. The first order differential equation to describe the operation of the RC network in figure 2.1.b is given in equation (2.6).

$$C_{lump}\frac{dV_{out}}{dt}+\frac{V_{out}-V_{in}}{R_d}=0 \tag{2.6}$$

The time constant (τ_d) of the network, which also represents the delay of the network, is calculated taking the driver resistance into account as,

$$\tau_d = R_d * C_{lump} \tag{2.7}$$

2.2.2.2 Lumped and Distributed RC Modeling

With technology scaling, the interconnect resistance begins to affect the signal characteristics and the simple lumped capacitance model discussed above becomes inadequate to represent such interconnect lines. A better model would be a lumped RC model, where the total interconnect resistance and capacitance of the interconnect are represented in terms of *R* and *C* respectively. Commonly used lumped models include *L*, Π and *T* networks as shown in figure 2.2 (Rabaey *et al.*, 2002).

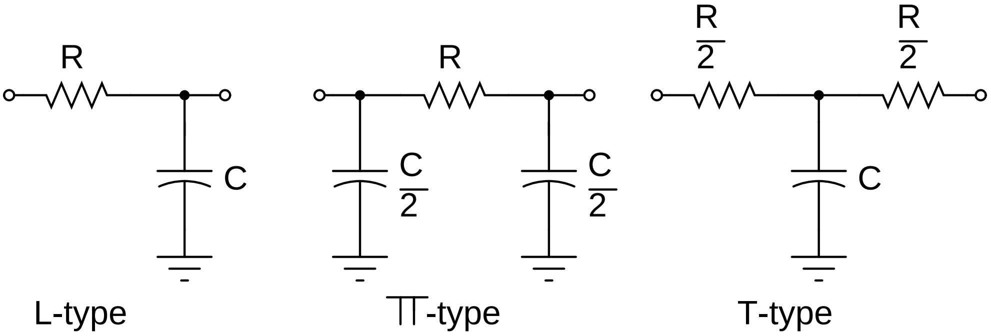


Figure 2.2: Lumped RC equivalent model

However, these models do not give accurate results in cases of long length interconnects (intermediate or global type) since the signal propagation delay along the interconnect is larger than the gate delay (Sakurai, 1993). In such cases, distributed RC networks of the type shown in figure 2.3 are used as interconnect equivalent circuits.

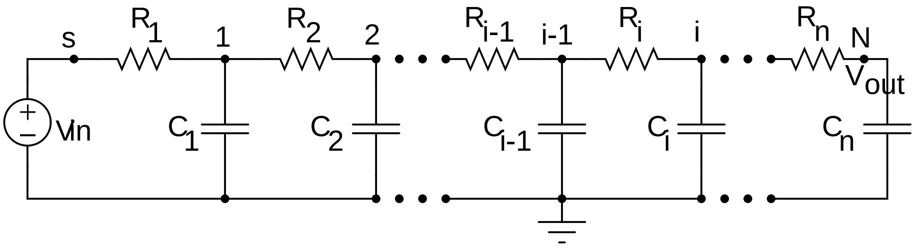


Figure 2.3: Distributed RC equivalent model

Distributed RC models for different types of long interconnects are discussed in (Sakurai, 1993). Deriving the expression for the output of networks consisting of large number of resistors and capacitors becomes very complex. To describe the behavior of such a network requires a set of differential equations possibly exhibiting multiple time-constants. Elmore delay is one of the simple alternative methods used to estimate the delay in such networks based on the first moment (Elmore, 1948). Elmore delay at node i in a circuit is given as

$$\tau_{di} = \sum_{k=1}^{N} R_{ik} C_k \tag{2.8}$$

where R_{ik} represents the resistance shared among the paths from the root node s to nodes k and i (applicable for the branched networks) while C_k represents the capacitance between node k in the network and ground. Both of these parameters represent per segment values of the interconnect. For a distributed RC network shown in figure 2.3, Elmore delay expression at node N can be written as

$$\tau_{dN} = \sum_{j=1}^{i} R_j \sum_{i=1}^{N} C_i = \sum_{i=1}^{N} R_{ii} C_i \tag{2.9}$$

and the delay at node i can be expressed as

$$\tau_{di} = R_1 C_1 + (R_1 + R_2) C_2 + \cdots\cdots + (R_1 + R_2 + \cdots + R_i) C_i \tag{2.10}$$

Considering that an interconnect of length L is partitioned into N identical segments, each segment having a length L/N, resistance rL/N and capacitance cL/N, the RC delay of the interconnect using the Elmore formula given in equation (2.10) can be expressed as

$$\tau_{dN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \cdots + Nrc) = rcL^2 \frac{N(N+1)}{2N^2} = RC \frac{N+1}{2N} \tag{2.11}$$

where R(=rL) and C(=cL) represents the total resistance and capacitance of the interconnect respectively. For very large values of N, equation (2.11) simplifies to

$$\tau_{dN} = \frac{RC}{2} = \frac{rcL^2}{2} \tag{2.12}$$

Equation (2.12) indicates that the interconnect delay is quadratic function of its length and that the delay of the distributed RC-line is one half of the delay that would have obtained by considering the lumped RC model.

As a design rule of thumb, *RC* network delay should be considered in the following conditions (Rabaey *et al.*, 2002).

1. Distributed RC network should be considered if the propagation delay of the wire (t_{pRC}) is much greater than the gate delay (t_{pgate}) (i.e. $t_{pRC} >> t_{pgate}$). This translates into equation (2.13) which determines the critical length (l_{crit}) of the interconnect line in-which RC delay becomes dominant.

   $$l_{crit} > \sqrt{\frac{t_{pgate}}{0.38rc}} \tag{2.13}$$

   where r and c represents the resistance and capacitance values per segment of the interconnect.

2. When rise (or fall) time of the source signal at the interconnect input is larger than the propagation delay of the interconnect, i.e., $t_{rise} > RC$, then the lumped capacitive model is sufficient to represent such lines.

2.2.2.3 Distributed RLC Modeling

For 0.25 μm technology and below, with increasing clock speeds and decreasing signal rise (or fall) times, on-chip inductive effects begin to show its impact on the delay behavior of the interconnects. Especially, inductive effects in intermediate/global interconnects are more severe because the reactive components become comparable to the resistive components of the interconnects. Further, with the adoption of low resistive Cu in place of Al, and the mutual inductance between the closely placed interconnects make the inductive effects more prominent (Banerjee and Mehrotra, 2002). Hence, traditional lumped or distributed RC models become inadequate and these models are replaced by distributed RLC models as shown in figure 2.4.

Inductance affects the interconnect performance in two ways (Banerjee and Mehrotra, 2002). Firstly, it affects the rise/fall time (slew rate) and signal delay through the interconnect . Secondly, in GHz regime, on-chip long interconnects behave as lossy distributed RLC transmission lines with the characteristic impedance of $Z_0 = \sqrt{(r+sl)/sc}$ where r, l, and c are per unit length resistance, inductance and capacitance values re-

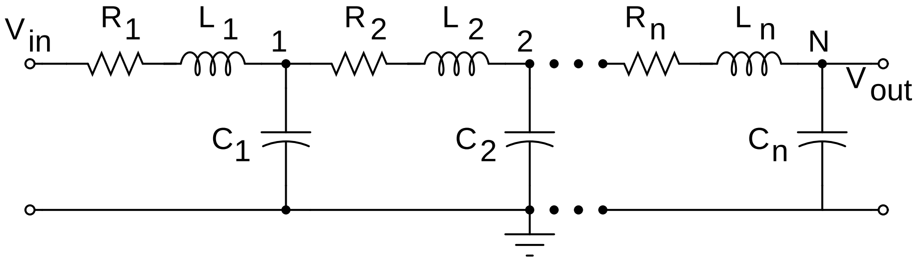


Figure 2.4: Distributed RLC equivalent model

spectively and s is the complex frequency ($j\omega$). If the series output impedance of the driver circuit and the input impedance of the interconnect is equal to Z_0, then no reflections occur at that junction. However, in practical VLSI circuits, the input impedance of the load is almost exclusively capacitive. Also, the transistors size in the driver circuit is optimized for minimum delay and its output impedance may not be equal to the characteristic impedance of the interconnect. In such circumstances, line inductance give rise to reflections which result in the overshoots and undershoots of the output voltage. Voltage overshoot causes reliability concerns whereas undershoot causes glitches and may result in false transitions at the output of the connected gate. Glitches increase the dynamic power dissipation while false transitions causes logic errors and severe timing violations. Expression to determine the interconnect length for which the inductive effects can not be ignored, is given by (Ismail *et al.*, 1999)

$$\frac{t_r}{2\sqrt{lc}} < length < \frac{2}{r}\sqrt{\frac{l}{c}} \tag{2.14}$$

where $length$ refers to the length of the interconnect segment. As a design rule of thumb, RLC models for the interconnects should be considered under the following conditions (Rabaey *et al.*, 2002).

1. Rise/fall time (t_r/t_f) of the input signal is less than 2.5 times flight time (t_{flight}) of the transmission line i.e. $t_r \leq 2.5 \times t_{flight}$.
2. Total resistance of the interconnect (R) is limited to $R < 5Z_0$.

2.2.2.4 Distributed RLGC Modeling

To capture high frequency effects such as undershoot, overshoot, ringing etc., interconnects are modeled as distributed RLC networks and the accuracy in interconnect performance estimation can be improved. Unfortunately, these distributed RC or RLC models lack in accuracy as the loss through the dielectric component (G) cannot be ignored in very high frequency (GHz) domains of the present VLSI designs (Ji *et al.*, 2009). With the increase in the speed of high performance VLSI circuits, inductance and conductance effects of interconnects are becoming more and more important. A distributed RLGC equivalent interconnect model is shown in figure 2.5 (Palit *et al.*, 2008).

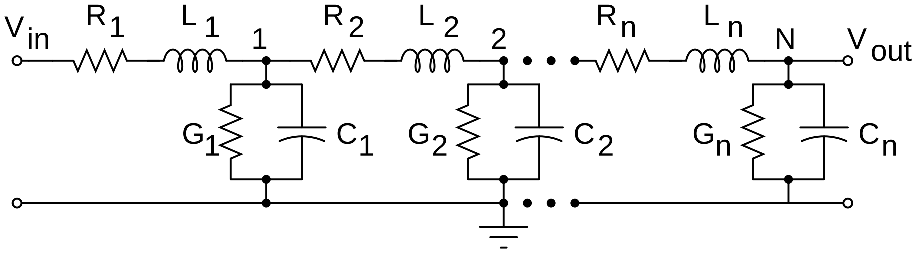


Figure 2.5: Distributed RLGC equivalent model

2.2.2.5 Analysis of Different Interconnect Equivalent Models

A comparison of the response for a step input signal based on different interconnect models (lumped C/lumped RC/distributed RC/lumped RLC/distributed RLGC network) is presented here. Table 2.1 shows the interconnect dimensions for different technology nodes ((ITRS, 2007) and (NIMG, 2008)). Interconnect parasitics, mutual inductance and coupling capacitance are calculated for the interconnect geometries given in table 2.1 using equations (1.3) to (1.13) for an interconnect length of 2.5 *mm*. Table 2.2 shows the interconnect parasitics calculated using these equations for different technology nodes.

Interconnect geometries of 65 *nm* technology node (table 2.1) are used to analyze the responses of the different interconnect equivalent models. The circuit for testing the

Table 2.1: Interconnect geometries for different technology nodes

Technology	Parameters	Value	Units
180 *nm*	Dielectric Constant(κ)	3.5	-
	Width (w)	900	*nm*
	Spacing (s)	900	*nm*
	Thickness (t)	2250	*nm*
	Dielectric Height (h)	650	*nm*
130 *nm*	Dielectric Constant(κ)	3.2	-
	Width (w)	650	*nm*
	Spacing (s)	650	*nm*
	Thickness (t)	1625	*nm*
	Dielectric Height (h)	450	*nm*
90 *nm*	Dielectric Constant(κ)	2.8	-
	Width (w)	460	*nm*
	Spacing (s)	460	*nm*
	Thickness (t)	1150	*nm*
	Dielectric Height (h)	300	*nm*
65 *nm*	Dielectric Constant(κ)	2.2	-
	Width (w)	450	*nm*
	Spacing (s)	450	*nm*
	Thickness (t)	1125	*nm*
	Dielectric Height (h)	200	*nm*
45 *nm*	Dielectric Constant(κ)	2.2	-
	Width (w)	135	*nm*
	Spacing (s)	135	*nm*
	Thickness (t)	270	*nm*
	Dielectric Height (h)	200	*nm*
32 *nm*	Dielectric Constant(κ)	2.2	-
	Width (w)	96	*nm*
	Spacing (s)	96	*nm*
	Thickness (t)	202	*nm*
	Dielectric Height (h)	150	*nm*

Table 2.2: Interconnect parasitics for different technology nodes

Interconnect Parameter	Technology Nodes						Units
	180 *nm*	130 *nm*	90 *nm*	65 *nm*	45 *nm*	32 *nm*	
R	27.16	52.07	103.97	108.64	1508.9	2830	Ω
L	3.935	4.098	4.27	4.282	4.96	5.113	*nH*
M	3.465	3.628	3.8	3.811	4.41	4.583	*nH*
C_g	801.17	760.59	701.48	763.07	253.66	229.97	fF
CC	964.24	876.62	760.94	567.96	561.44	559.91	fF
C_{total}	2.72	2.51	2.22	1.89	1.376	1.34	*pF*
G	144.2	98.876	64.5	68.67	6.84	4.414	$\mu\mho$

different interconnect equivalent models is shown in figure 2.6. In this set-up, interconnect equivalent model is driven by a step signal (t_r=10 *ps*) with a source resistance R_s of 50 Ω and a capacitive load C_L of 500 fF at the output node.

Figure 2.7 shows the response of the different interconnect equivalent models. These

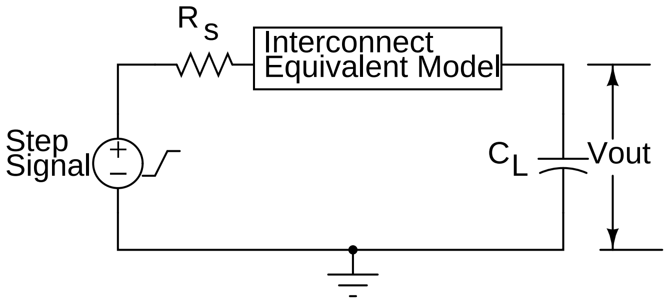


Figure 2.6: Circuit for testing the response of different interconnect models

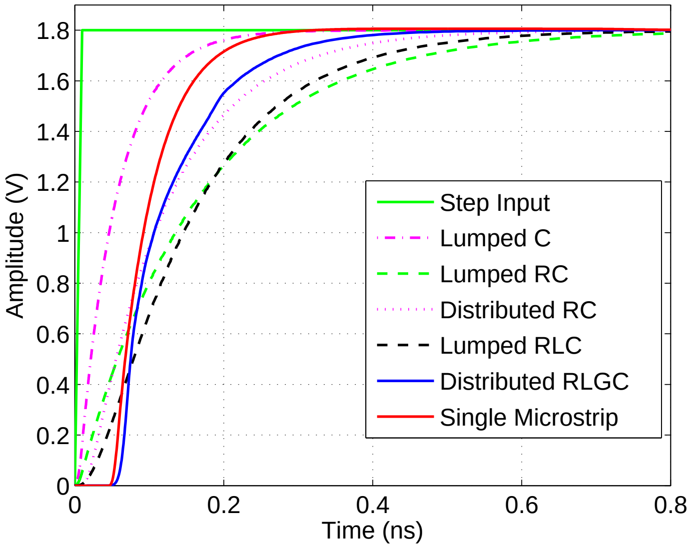


Figure 2.7: SPICE response of different interconnect models

responses are compared with the microstrip layout response of a single interconnect line. From the graph, it can be seen that the RLGC distributed model response is closest to the microstrip layout response. Thus, the distributed RLGC model best approximates the interconnect line and hence it is used for further analysis of the on-chip intermediate/global interconnect metal lines.

2.2.3 Discussion on Previously used Interconnect Delay Models

Over the years, the equivalent models used to represent the interconnects are chosen based on the frequencies used for the circuit operation. Initially, interconnects are modeled as lumped RC and later as distributed RC networks. In branched or distributed

RC networks, delay is estimated using Elmore delay models based on the first moments (Elmore, 1948). In (Horowitz, 1983), accuracy of the delay model is improved by estimating the first and second moments. In (Pillage and Rohrer, 1990), it is shown that the accuracy of the estimated delay improves further by determining the model from the higher order moments. When the operating frequencies reach GHz regime, inductive effects become prominent and influence the interconnects delay behavior. But the above mentioned models fail to capture the inductive effects in estimating the delay of the interconnects (Banerjee and Mehrotra, 2002).

Second and higher order RLC models of the interconnect provided significant improvements over the accuracy of first-order RC delay models. This is so because RLC trees and higher order transfer functions have oscillatory output voltages and are thus able to predict increased delays due to increased settling times of interconnect voltages. An analytical delay model based on first and second moments of distributed RLC network is presented in (Kahng and Muddu, 1997). This model considered the effects of inductance and hence the resulting delay estimation is significantly better than Elmore delay model. This model is further improved by (Zhou *et al.*, 2008) by replacing each interconnect segment with its equivalent ABCD matrix and delay is estimated from the first two moments of the circuit. Around the same time, a new delay model is proposed by (Kim and Wong, 2007) to improve the accuracy using Effective Distance Correction Factor (EDCF) to consider the resistive shielding of downstream capacitance. This model is derived by considering the input rise time while retaining the efficiency and simplicity of the Elmore delay model.

A distributed RC interconnect model based on time domain response using Partial Differential Equations (PDE) is presented in (Sakurai, 1993). Similar results using compact distributed RLC network models are presented in (Davis and Meindl, 2000; Venkatesan *et al.*, 2003*a*) and (Venkatesan *et al.*, 2003*b*). Analytical delay model for RLC networks for a ramp input is presented in (Ren *et al.*, 2007) and (Kim and Wong, 2007) while in (Chen and Friedman, 2005), a RLC interconnect model based on Fourier analysis is presented. This method helps in determining the timing characteristics of the signal in the early stages of circuit level design. Closed form delay expressions based on current mode signaling is derived in (Aswatha *et al.*, 2008) and it is shown that this modeling approach is more efficient when compared with the voltage mode signaling methods. In (Kang *et al.*, 2005), expression for the transfer function of the distributed RLGC model with arbitrary source impedance and unmatched load is derived with on-chip global interconnect boundary conditions. In this paper, the effects of including conductance in the model is analyzed by comparing the response with other model responses. In (Palit *et al.*, 2008), distributed RLGC transient model of coupled interconnects is used for crosstalk noise analysis. The effect of scaling on R, L, G and C parameters is derived in (Jun-De JIN *et al.*, 2008). In (Vande Ginste *et al.*, 2011), accurate broadband macro-models are conceived by means of adaptive frequency sampling.

In recent years, algorithms based on the time domain analysis of substrate integrated interconnect structures have been developed. Finite-Element Time-Domain (FETD) is one such algorithm introduced for the solution of time-dependent electromagnetic field analysis of the interconnects (Du *et al.*, 2008). This algorithm has the advantage of higher accuracy and lower dispersion errors as compared to the Finite-Difference Time-Domain (FDTD) method. In FETD method, matrix equation needs to be solved at each time step in the simulation. This potentially requires extensive computational resources for the analysis of large problems, both in terms of memory and floating-point operations. Present generation high-performance parallel computers can provide these computational resources, but these resources cannot be fully exploited using traditional sequential algorithms for solving matrix equations which can be highly inefficient on parallel computers.

The Finite-Element Tearing and Interconnecting (FETI) algorithm presents an alternative method to solve the matrix equation. It enforces the field continuity explicitly along the edge shared by more than two sub-domains and implicitly at the interfaces between two subdomains through the use of Lagrange multipliers (Li and Jin, 2007). This method is found to be extremely efficient for problems with geometric repetitions. Even though these methods are accurate, they are highly complex and computationally intensive.

2.2.3.1 Choice of RLGC Modeling using State Space Approach

Different electrical level models lead to different effects being modeled and accuracy being traded off for computational complexity. In heterogeneous media such as layered dielectrics, the propagation mode is not restricted to the TEM mode. However if the separation of the conductors is small compared to the wavelengths, which is generally in a chip, approximate Transverse Electro Magnetic (TEM) propagation exists. Assuming TEM propagation, all wires can be generalized to transmission lines which have series resistance and inductance, and parallel capacitance and conductance. All other models are simplifications of the general transmission line. In most of the modeling methods discussed in section 2.2.3, conductance effect of the interconnects is neglected. When the switching speed of the signals reach GHz frequencies, the losses in the dielectric component cannot be neglected. In view of the above, a RLGC based interconnect model using state space approach is presented in this section.

In DSM regime, on-chip interconnects are closely placed and have Manhattan geometries. For an efficient design, the estimation of interconnect metrics is to be done early in the design cycle and hence there is a need for a modular approach in determining the various interconnect metrics and coupling effects based on the length and geometry of the interconnects. Up until now, most papers have confined the coupling effects only to the adjacent lines in a given metal layer, while coupling across metal layers is mostly ignored. Further, the inductive and capacitive coupling effects between the branched segments of an interconnect are completely ignored. Neglecting these effects would lead to inaccurate models and in-turn result in inaccurate estimation of the interconnect metrics.

In this work, the different metrics for any arbitrary length and coupling of interconnect represented by an RLGC model is determined using state space approach. The state space representation is modular in nature and offers greater flexibility in determining the metrics for a variety of interconnect geometries. First, the state space matrices are derived for Single and Two-Coupled interconnects. Later, this approach is extended to **L** and **T** shaped interconnect lines so as to include the coupling effects within the branched segments of the same interconnect. Generalized state space models are derived for the single, coupled, **L** and **T** type of interconnects. While deriving these generalized models, it is assumed that each distributed RLGC network has ‘n’ segments. Using these models, interconnect network having arbitrary Manhattan geometry can be modeled.

2.3 State Space Approach to RLGC Network Modeling

At high frequencies of operation with sub-nanosecond rise times, the length and cross section of an interconnect can become a significant fraction of the operating wavelength and field components in the direction of propagation can no longer be neglected (Achar, 2011). In such a scenario, interconnects can be treated as transmission lines (Microstrip layers). A uniform single interconnect system of length l is shown in figure 2.8. An infinitesimally small section (Δx) at any position x along the interconnect can be modeled as a lumped RLGC circuit as shown in figure 2.9.

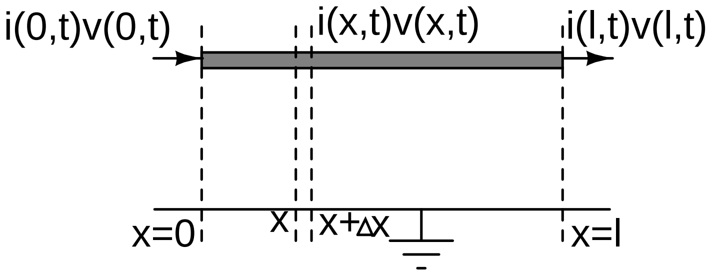


Figure 2.8: A simple interconnect line system

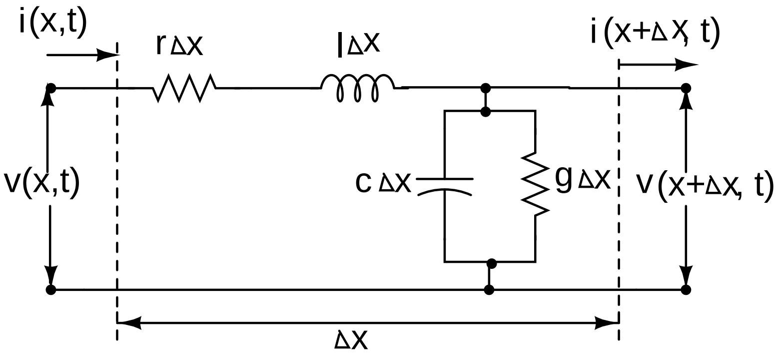


Figure 2.9: Equivalent circuit of an infinitesimal section

The energy stored in the magnetic field for an infinitesimal section Δx of the wire is represented by a series inductance ($l\Delta x$). The shunt capacitance ($c\Delta x$) represents the energy stored in the electric field between the signal conductor and the underlying return path. The signal loss effect in the transmission line is modeled by including series resistance ($r\Delta x$) and shunt conductance ($g\Delta x$). Applying Kirchhoffs laws to the circuit shown in figure 2.9, we get (Paul, 2008),

$$\frac{v(x+\Delta x,t)-v(x,t)}{\Delta t} = -ri(t) - l\frac{\partial i(t)}{\partial t} \tag{2.15}$$

$$\frac{i(x+\Delta x,t)-i(x,t)}{\Delta t} = -gv(t) - c\frac{\partial v(t)}{\partial t} \tag{2.16}$$

Letting $\Delta x \rightarrow 0$, the above equations become

$$\frac{\partial v(t)}{\partial t} = -\left[ri(t) + l\frac{\partial i(t)}{\partial t}\right] \tag{2.17}$$

$$\frac{\partial i(t)}{\partial t} = -\left[gv(t) + c\frac{\partial v(t)}{\partial t}\right] \tag{2.18}$$

Applying Laplace transformation to equations (2.17) and (2.18) and results in

$$sV(s) = -[r+sl]I(s) \tag{2.19}$$

$$sI(s) = -[g+sc]V(s). \tag{2.20}$$

2.3.1 General State Space Model of a System

State space description provides the dynamics of the system as a set of coupled differential equations in terms of internal variables (known as state variables) together with a set of algebraic equations that combine the state variables into physical output variables. The state variables give the internal description of the system which completely characterizes the state of the system at any time t (Li and Pileggi, 2003). Block diagram of a system having p input variables ($u_1(t)$ to $u_p(t)$), n state variables ($x_1(t)$ to $x_n(t)$), and q output variables ($y_1(t)$ to $y_q(t)$) as shown in figure 2.10. The state of the system

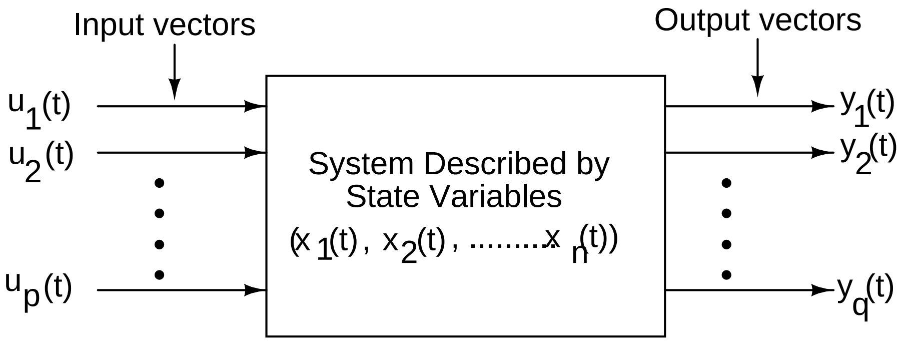


Figure 2.10: System with inputs and outputs

is determined based on following conditions :

- Initial values of the state variables at time t=0.
- Magnitude of the input signals should be zero for $t<0$.

From these conditions, any output variable ($y_i(t)$) can be computed using the state variables. A linear time invariant network containing resistors, inductors, capacitors with p inputs, q outputs and n state variables can be written in the following form:

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t)+\mathbf{B}\mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}\mathbf{x}(t)+\mathbf{D}\mathbf{u}(t) \end{aligned} \tag{2.21}$$

where dim$[\mathbf{A}(\cdot)]$=$n\times n$, dim$[\mathbf{B}(\cdot)]$=$n\times p$, dim$[\mathbf{C}(\cdot)]$=$q\times n$, dim$[\mathbf{D}(\cdot)]$=$q\times p$, dim$[\mathbf{x}(\cdot)]$=$n\times 1$, dim$[\mathbf{y}(\cdot)]$=$q\times 1$ and $\dot{\mathbf{x}}(t) := \dfrac{d\mathbf{x}(t)}{dt}$.

In equation (2.21), $\mathbf{x}(\cdot)$ is the state vector, $\mathbf{y}(\cdot)$ is the output vector, $\mathbf{u}(\cdot)$ is the input (or control) vector, $\mathbf{A}(\cdot)$is the state matrix, $\mathbf{B}(\cdot)$ is the input matrix, $\mathbf{C}(\cdot)$ is the output matrix and $\mathbf{D}(\cdot)$ is the feedthrough (or feedforward) matrix.

2.3.1.1 Procedure to find the State Space Matrices of an Interconnect Line

Following steps outline the procedure to determine the state space matrices for an interconnect line.

1. Interconnect lines are represented by distributed RLGC network. In the proposed model, state space matrices are represented in terms of per segment values of re-

sistance, inductance, capacitance, conductance, mutual inductance and coupling capacitance.

2. State variables of the system are described by inductor currents and capacitor voltages. If the RLGC network is modeled as having *n* segments (*n* inductors and *n* capacitors), then there will be *2n* state variables in the system.
3. Nodal and loop equations containing capacitor voltages and inductor currents are obtained and expressed as matrices.
4. Elements of matrix E represents the capacitive and inductive coupling.
5. Elements of matrix A represents resistance and conductance.
6. Matrices B, C and D represents input, output and feedthrough parameters.

In case of RLGC network nodes that are inductively and capacitively coupled, deriving the state space matrices given in equation (2.21) becomes a bit cumbersome. In such cases, Descriptor state equations can be used as given below.

$$\begin{aligned}\mathbf{E}\dot{\mathbf{x}}(t) &= \mathbf{A_d}\mathbf{x}(t)+\mathbf{B_d}\mathbf{u}(t)\\ \mathbf{y}(t) &= \mathbf{C}\mathbf{x}(t)+\mathbf{D}\mathbf{u}(t) \qquad (2.22)\end{aligned}$$

where $\mathbf{A}$=$\mathbf{E}^{-\mathbf{1}}\mathbf{A_d}$ and $\mathbf{B}$=$\mathbf{E}^{-\mathbf{1}}\mathbf{B_d}$

Further, since there is no direct coupling between input and output, feedforward matrix will be equal to zero i.e. $\mathbf{D}$ = 0. Depending upon *p* and *q* values, the system is SISO (Single Input Single Output) or MIMO (Multiple Input Multiple Output).

2.3.1.2 Segmenting Interconnect Line for Accurate Modeling

Minimum number of RLGC segments required to model the interconnect line of length *l* is given as (Hall *et al.*, 2000)

$$N_{\min} \geq \frac{10 \cdot l}{t_r v} \qquad (2.23)$$

where v is the propagation speed of the signal in the interconnect and t_r is the rise time of the signal. N_{min} for 2.5 *mm* interconnect line at 65 *nm* technology node is found to be 15 for a t_r of 10 *ps* (as per equation (2.23)).

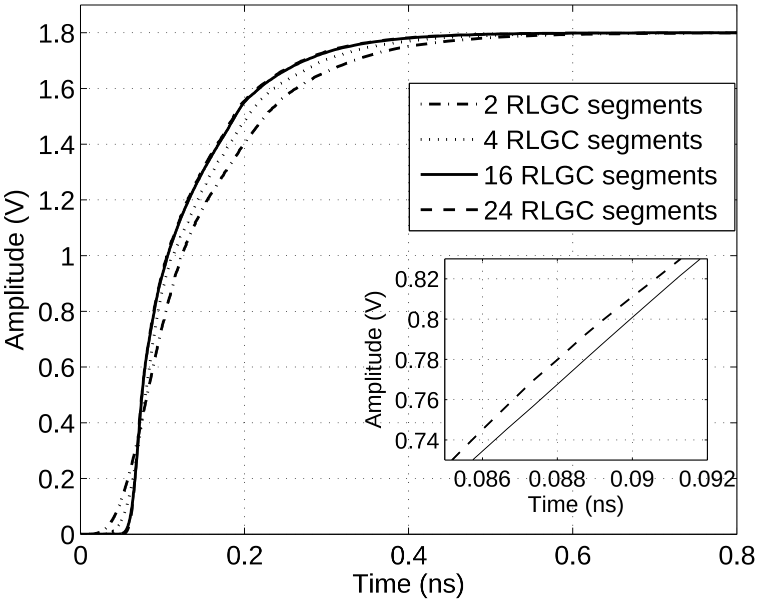


Figure 2.11: Effect of the number of segments used on step response for the distributed RLGC modeling

SPICE simulation (using Cadence) of 2.5 *mm* interconnect line at 65 *nm* technology considering different number of segments is performed and the results are plotted in figure 2.11. From the figure, it can be seen that, simulating the interconnect line by segmenting it by fewer number than the one obtained from equation (2.23) results in inaccurate response. Hence, in all the simulations that follow, the number of sections considered for a given length of interconnect line is computed using equation (2.23).

2.4 Proposed models

In this section, generalized distributed RLGC networks for single, coupled, **L** and **T**-type of interconnects are discussed. Figure 2.12 shows the 3D view of the single, coupled, **L** and **T** type of interconnects considered for modeling. Generalized state space matrices are derived using procedure given in section 2.3.1.1 in each case. In the state space representation, matrix **E** represents the distributed capacitive and inductive elements while matrix **A** represents the distributed resistive and conductive elements. The size of the matrices **E** and **A** depend on the total number of state variables present in the

RLGC interconnect network.

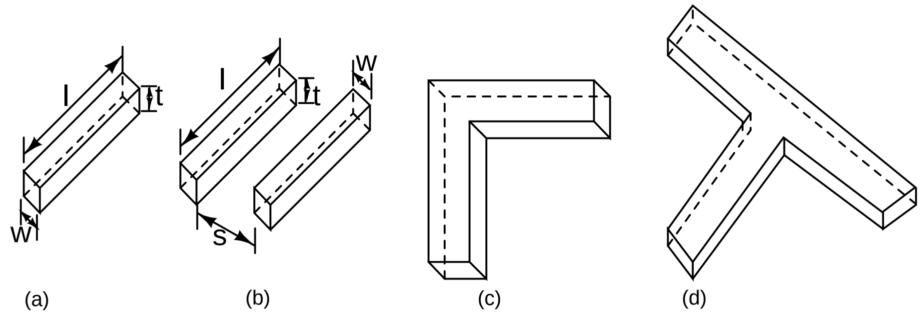


Figure 2.12: Structures of different interconnect types: (a) Single (b) Coupled (c) **L**-section and (d) **T**-section

2.4.1 Generalized State Space Model of a Single Interconnect Line

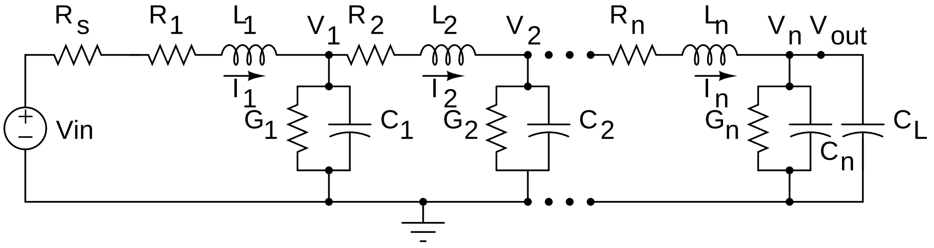


Figure 2.13: Generalized RLGC model of the single interconnect line

Figure 2.12(a) shows the 3D view of an isolated single interconnect line and figure 2.13 shows its equivalent distributed RLGC network. State variables associated with the capacitors (V_1, V_2, $\cdots$, V_n) and inductors (I_1, I_2, $\cdots$, I_n) in the network are shown in figure 2.13. Resistance, inductance, conductance and capacitance of i^{th} segment in this model are represented by R_i, L_i, G_i and C_i respectively where i=1, 2,$\cdots\cdots$, n. The generalized state matrices **E** and **A** for a n segment case is given by

$$\mathbf{E} = \begin{bmatrix} \mathbf{E_{11}} & \mathbf{0} \\ \mathbf{0} & \mathbf{E_{22}} \end{bmatrix} \tag{2.24}$$

$$\mathbf{A} = \begin{bmatrix} \mathbf{A_{11}} & \mathbf{A_{12}} \\ \mathbf{A_{21}} & \mathbf{A_{22}} \end{bmatrix} \tag{2.25}$$

In equations (2.24) and (2.25), every element is a matrix whose size depends on the number of capacitive (or inductive) state variables present in the RLGC network. The matrix structure of the elements in equations (2.24) and (2.25) are given below.

$$E_{11} = \begin{bmatrix} L_1 & 0 & \cdots & 0 \\ 0 & L_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & L_n \end{bmatrix}$$

$$E_{22} = \begin{bmatrix} C_1 & 0 & \cdots & 0 \\ 0 & C_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & C_n \end{bmatrix}$$

$$A_{11} = \begin{bmatrix} -R_1 & 0 & \cdots & 0 \\ 0 & -R_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & -R_n \end{bmatrix}$$

$$A_{12} = \begin{bmatrix} -1 & 0 & \cdots & \cdots & 0 \\ 1 & -1 & 0 & \cdots & 0 \\ 0 & \ddots & \ddots & \cdots & 0 \\ \vdots & \vdots & \ddots & \ddots & 0 \\ 0 & 0 & \cdots & 1 & -1 \end{bmatrix}$$

$$A_{21} = \begin{bmatrix} 1 & -1 & 0 & \cdots & 0 \\ 0 & 1 & -1 & \cdots & 0 \\ 0 & 0 & \ddots & \ddots & 0 \\ \vdots & \vdots & \vdots & \ddots & -1 \\ 0 & 0 & \cdots & 0 & 1 \end{bmatrix}$$

$$A_{22} = \begin{bmatrix} -G_1 & 0 & \cdots & 0 \\ 0 & -G_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & -G_n \end{bmatrix}$$

State space model and SPICE response of a single interconnect line of length 2.5 *mm*

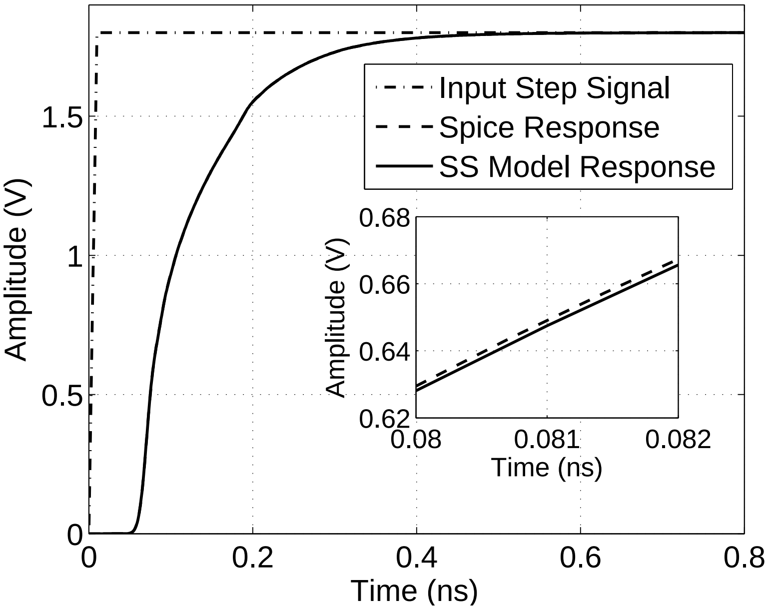


Figure 2.14: Comparison of the state space model and SPICE responses of the single interconnect line

(figure 2.13) for a step input signal is shown in figure 2.14. The model response is exactly matching with the SPICE response. The inset plot in figure 2.14 shows the closeness of the model and SPICE response.

2.4.2 Generalized State Space Model of Coupled Interconnect Lines

Figure 2.12(b) shows the 3D view of two closely placed interconnect lines and figure 2.15 shows its equivalent RLGC network. State variables associated with the capacitors

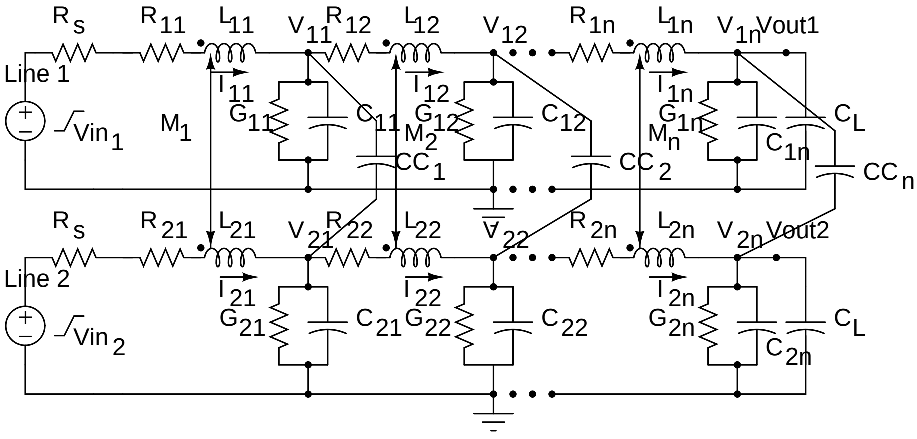


Figure 2.15: Generalized RLGC model of the coupled interconnect lines

(V_{11} to V_{1n} and V_{21} to V_{2n}) and inductors (I_{11} to I_{1n} and I_{21} to I_{2n}) in Line 1 and Line 2 are shown in figure 2.15. Resistance, inductance, conductance and capacitance of an i^{th} segment in the model of Line 1 and Line 2 are represented by R_{1i}, L_{1i}, G_{1i}, C_{1i}, R_{2i}, L_{2i}, G_{2i} and C_{2i} respectively. To model the coupling effects between closely placed lines (Line 1 and Line 2 in this case), consider the mutual inductance (M_i) and coupling capacitances (CC_i) between the coupled lines as shown in figure 2.15. The generalized state space matrices are given as

$$\mathbf{E_{coup}} = \begin{bmatrix} \mathbf{E_{C11}} & \mathbf{E_{C12}} & \mathbf{0} & \mathbf{0} \\ \mathbf{E_{C21}} & \mathbf{E_{C22}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{E_{C33}} & \mathbf{E_{C34}} \\ \mathbf{0} & \mathbf{0} & \mathbf{E_{C43}} & \mathbf{E_{C44}} \end{bmatrix} \tag{2.26}$$

$$\mathbf{A_{coup}} = \begin{bmatrix} \mathbf{A_{C11}} & \mathbf{0} & \mathbf{A_{C13}} & \mathbf{0} \\ \mathbf{0} & \mathbf{A_{C22}} & \mathbf{0} & \mathbf{A_{C24}} \\ \mathbf{A_{C31}} & \mathbf{0} & \mathbf{A_{C33}} & \mathbf{0} \\ \mathbf{0} & \mathbf{A_{C42}} & \mathbf{0} & \mathbf{A_{C44}} \end{bmatrix} \tag{2.27}$$

In equations (2.26) and (2.27), every element is a matrix whose size depends on the number of capacitive (or inductive) state variables present in one RLGC line of the coupled interconnect network. The generalized matrix structures of the elements in equations (2.26) and (2.27) are given below.

$$\mathbf{E_{C11}} = \begin{bmatrix} L_{11} & 0 & \cdots & 0 \\ 0 & L_{12} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & L_{1n} \end{bmatrix}$$

$$\mathbf{E_{C12}} = \mathbf{E_{C21}} = \begin{bmatrix} M_1 & 0 & \cdots & 0 \\ 0 & M_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & M_n \end{bmatrix}$$

$$\mathbf{E_{C22}} = \begin{bmatrix} L_{21} & 0 & \cdots & 0 \\ 0 & L_{22} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & L_{2n} \end{bmatrix}$$

$$\mathbf{E_{C33}} = \begin{bmatrix} C_{11}+CC_1 & 0 & \cdots & 0 \\ 0 & C_{12}+CC_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & C_{1n}+CC_n \end{bmatrix}$$

$$\mathbf{E_{C34}} = \mathbf{E_{C43}} = \begin{bmatrix} -CC_1 & 0 & \cdots & 0 \\ 0 & -CC_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & -CC_n \end{bmatrix}$$

$$\mathbf{E_{C44}} = \begin{bmatrix} C_{21}+CC_1 & 0 & \cdots & 0 \\ 0 & C_{22}+CC_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & C_{2n}+CC_n \end{bmatrix}$$

$$\mathbf{A_{C11}} = \begin{bmatrix} -R_{11} & 0 & \cdots & 0 \\ 0 & -R_{12} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & -R_{1n} \end{bmatrix}$$

$$\mathbf{A_{C13}} = \mathbf{A_{C24}} = \begin{bmatrix} -1 & 0 & \cdots & 0 \\ 1 & -1 & \cdots & 0 \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 1 & -1 \end{bmatrix}$$

$$\mathbf{A_{C22}} = \begin{bmatrix} -R_{21} & 0 & \cdots & 0 \\ 0 & -R_{22} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & -R_{2n} \end{bmatrix}$$

$$\mathbf{A_{C31}} = \mathbf{A_{C42}} = \begin{bmatrix} 1 & -1 & 0 & \cdots & 0 \\ 0 & 1 & -1 & \cdots & 0 \\ 0 & 0 & \ddots & \ddots & \vdots \\ 0 & \cdots & 0 & 0 & 1 \end{bmatrix}$$

$$\mathbf{A_{C33}} = \begin{bmatrix} -G_{11} & 0 & \cdots & 0 \\ 0 & -G_{12} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & -G_{1n} \end{bmatrix}$$

$$\mathbf{A_{C44}} = \begin{bmatrix} -G_{21} & 0 & \cdots & 0 \\ 0 & -G_{22} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & -G_{2n} \end{bmatrix}$$

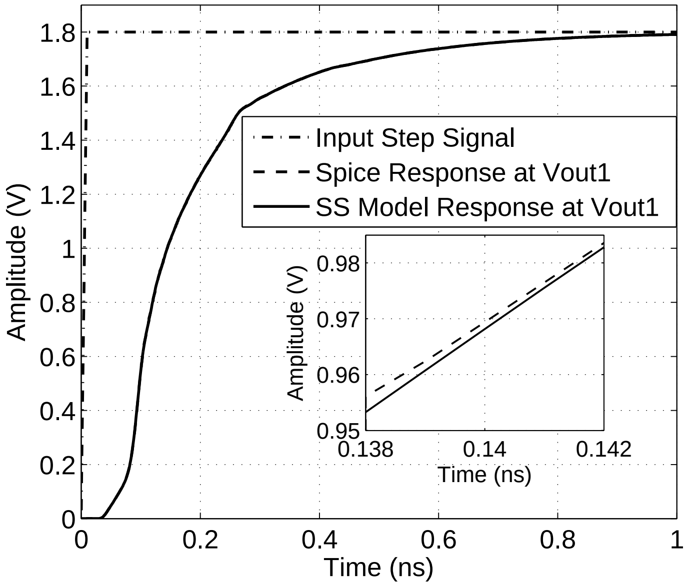


Figure 2.16: Comparison of the state space model and SPICE responses of the coupled interconnects at V_{out1} of Line 1

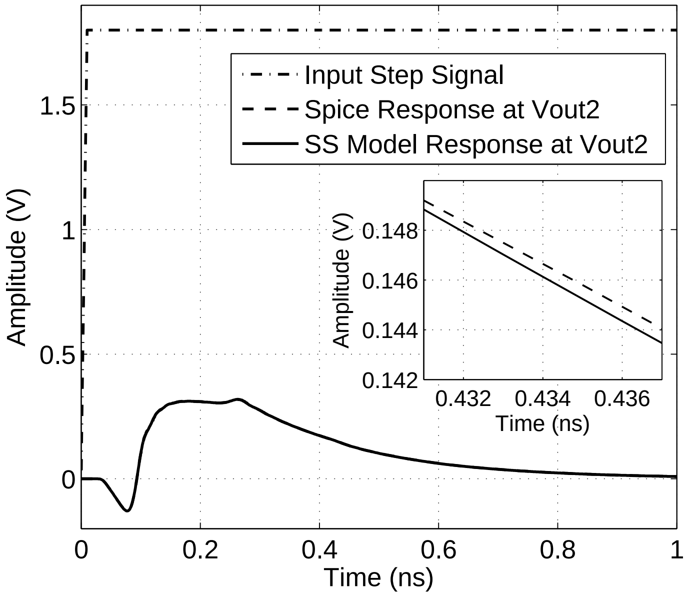


Figure 2.17: Comparison of state space model and SPICE responses of the coupled interconnects at V_{out2} of Line 2

To validate our model, a step signal of voltage 1.8 V is applied at one end of Line 1 and the output (SPICE response) at the other end of Line 1 and Line 2 is measured. Figures 2.16 and 2.17 shows the SPICE response along with the state space model response for Line 1 and Line 2 respectively. In both the cases, model and SPICE responses are closely matching (see inset figure).

2.4.3 Generalized State Space Model of an L-section

A **L**-section of the interconnect structure and its equivalent generalized RLGC model are shown in figures 2.12(c) and 2.18 respectively. The left and right wing of the interconnect line are named as m and p respectively. Each wing of the model is considered to have n segments. Resistance, inductance, conductance and capacitances of the left and the right wing are represented by subscripts m and p respectively while the coupling capacitance and mutual inductance between i^{th} segment in the left wing and j^{th} segment in the right wing are represented by the subscripts CC_{ij} and M_{ij} respectively. State variables associated with the capacitors (V_{m1} to V_{mn} and V_{p1} to V_{pn}) and inductors (I_{m1} to I_{mn} and I_{p1} to I_{pn}) in the left and right wings are shown in figure 2.18.

The generalized state matrices **E** and **A** are derived and expressed as

$$\mathbf{E_{Lsect}} = \begin{bmatrix} \mathbf{E_{L11}} & \mathbf{E_{L12}} & \mathbf{0} & \mathbf{0} \\ \mathbf{E_{L21}} & \mathbf{E_{L22}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{E_{L33}} & \mathbf{E_{L34}} \\ \mathbf{0} & \mathbf{0} & \mathbf{E_{L43}} & \mathbf{E_{L44}} \end{bmatrix} \tag{2.28}$$

$$\mathbf{A_{Lsect}} = \begin{bmatrix} \mathbf{A_{L11}} & \mathbf{0} & \mathbf{A_{L13}} & \mathbf{0} \\ \mathbf{0} & \mathbf{A_{L22}} & \mathbf{0} & \mathbf{A_{L24}} \\ \mathbf{A_{L31}} & \mathbf{0} & \mathbf{A_{L33}} & \mathbf{0} \\ \mathbf{0} & \mathbf{A_{L42}} & \mathbf{0} & \mathbf{A_{L44}} \end{bmatrix} \tag{2.29}$$

For the convenience of deriving the state space matrices, equal number of RLGC segments are considered in the left and right wing of the **L** interconnect structure (figure 2.18). In equations (2.28) and (2.29), every element is a matrix whose size depends on

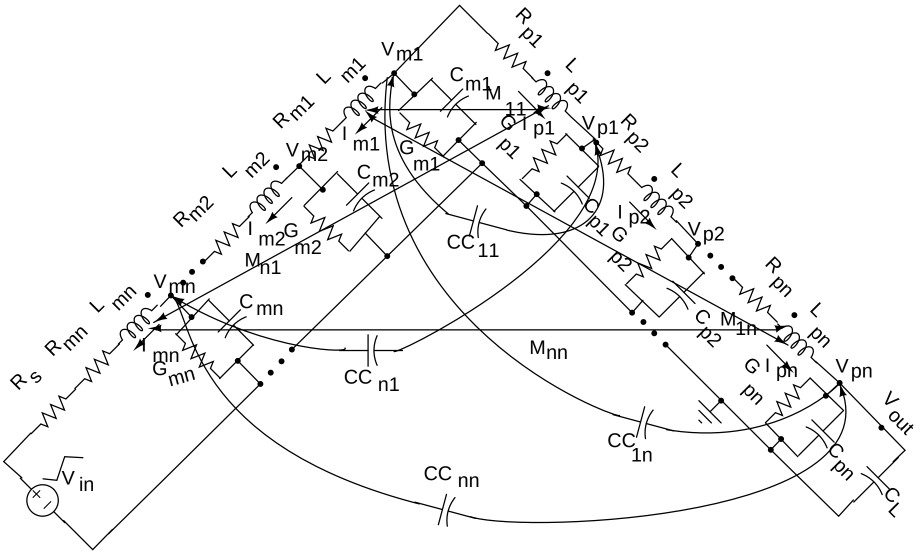


Figure 2.18: Generalized RLGC model of the L-section line

the number of capacitive (or inductive) state variables present in the left (or right) wing of the RLGC interconnect network. The generalized matrix structures of the elements in equations (2.28) and (2.29) are given below.

$$\mathbf{E_{L11}} = \begin{bmatrix} 0 & \cdots & 0 & L_{mn} \\ 0 & \cdots & L_{m(n-1)} & 0 \\ \vdots & \iddots & \vdots & \vdots \\ L_{m1} & \cdots & 0 & 0 \end{bmatrix}$$

$$\mathbf{E_{L12}} = \mathbf{E_{L21}} = \begin{bmatrix} M_{1n} & M_{2n} & \cdots & M_{nn} \\ M_{1(n-1)} & M_{2(n-1)} & \cdots & M_{n(n-1)} \\ \vdots & \vdots & \vdots & \vdots \\ M_{11} & M_{21} & \cdots & M_{n1} \end{bmatrix}$$

$$\mathbf{E_{L22}} = \begin{bmatrix} L_{p1} & 0 & \cdots & 0 \\ 0 & L_{p2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & L_{pn} \end{bmatrix}$$

$$\mathbf{E_{L33}} = \begin{bmatrix} 0 & \cdots & 0 & C_{mn}+CC_{kn} \\ 0 & \cdots & C_{m(n-1)}+CC_{k(n-1)} & 0 \\ \vdots & \iddots & \vdots & \vdots \\ C_{m1}+CC_{k1} & \cdots & 0 & 0 \end{bmatrix}$$

$$\mathbf{E_{L34}} = \mathbf{E_{L43}} = \begin{bmatrix} -CC_{1n} & -CC_{2n} & \cdots & -CC_{nn} \\ -CC_{1(n-1)} & -CC_{2(n-1)} & \cdots & -CC_{n(n-1)} \\ \vdots & \vdots & \vdots & \vdots \\ -CC_{11} & -CC_{21} & \cdots & -CC_{n1} \end{bmatrix}$$

$$\mathbf{E_{L44}} = \begin{bmatrix} C_{p1}+CC_{1k} & 0 & \cdots & 0 \\ 0 & C_{p2}+CC_{2k} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & C_{pn}+CC_{nk} \end{bmatrix}$$

$$\mathbf{A_{L11}} = \begin{bmatrix} 0 & \cdots & 0 & -R_{mn} \\ 0 & \cdots & -R_{m(n-1)} & 0 \\ \vdots & \iddots & \vdots & \vdots \\ -R_{m1} & \cdots & 0 & 0 \end{bmatrix}$$

$$\mathbf{A_{L13}} = \begin{bmatrix} 0 & \cdots & 0 & 1 \\ 0 & \cdots & -1 & 1 \\ \vdots & \iddots & \iddots & \vdots \\ 1 & -1 & \cdots & 0 \end{bmatrix}$$

$$\mathbf{A_{L22}} = \begin{bmatrix} -R_{p1} & 0 & \cdots & 0 \\ 0 & -R_{p2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & \cdots & 0 & -R_{pn} \end{bmatrix}$$

$$\mathbf{A_{L24}} = \begin{bmatrix} -1 & 0 & \cdots & 0 \\ 1 & -1 & \cdots & 0 \\ \vdots & \iddots & \iddots & \vdots \\ 0 & 0 & \cdots & -1 \end{bmatrix}$$

$$\mathbf{A_{L31}} = \begin{bmatrix} 0 & \cdots & 0 & 1 & -1 \\ 0 & \cdots & -1 & 1 & 0 \\ \vdots & \iddots & \iddots & \vdots & \vdots \\ -1 & 0 & \cdots & 0 & -1 \end{bmatrix}$$

$$\mathbf{A_{L33}} = \begin{bmatrix} -G_{m1} & 0 & \cdots & 0 \\ 0 & -G_{m2} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & -G_{mn} \end{bmatrix}$$

$$\mathbf{A_{L44}} = \begin{bmatrix} -G_{p1} & 0 & \cdots & 0 \\ 0 & -G_{p2} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & -G_{pn} \end{bmatrix}$$

Applying a signal of voltage 1.8 V at one end of the **L** shaped structure, the response at the other end is measured. The SPICE and state space responses are then plotted in figure 2.19 and are found to be closely matching.

2.4.3.1 Mutual Inductance and Coupling Capacitance Values between the Nodes of L Structure

In the generalized RLGC model of the **L**-structure shown in figure 2.18, mutual inductance (M) and coupling capacitance (CC) from every node in the left wing to all the nodes of the right wing are taken into consideration while deriving the state space ma-

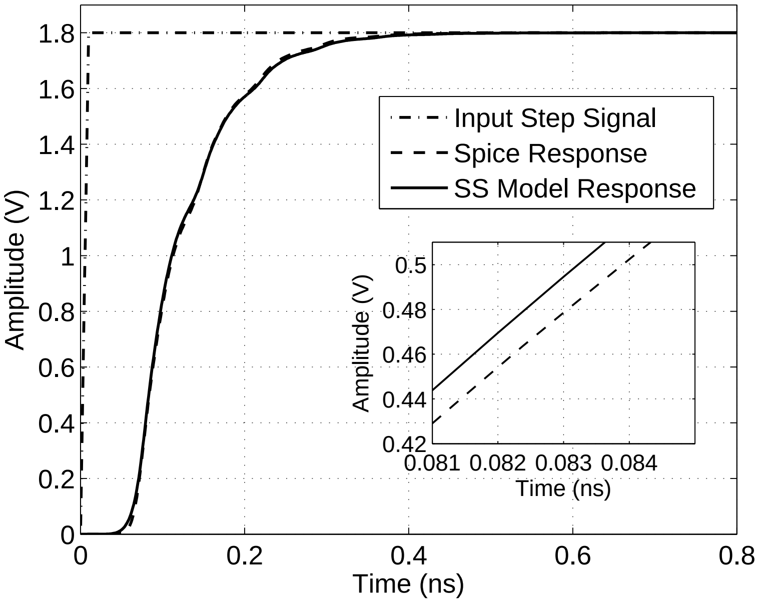


Figure 2.19: Comparison of state space model and SPICE responses of the **L** section

trices. The *M* and *CC* values vary with distance between the nodes and are calculated using equations (1.9) and (1.11). To find the relative percentage change in M and CC values from one of the nodes in the left wing to all the nodes in the right wing, diagonal distance between the the nodes are calculated. Table 2.3 shows a particular case of the relative percentage change in the values of *M* and *CC* for the distance between the first node of the left wing to all the nodes of the right wing (*p*1 to *m*1, *p*1 to *m*2 and so on in figure 2.18).

Table 2.3 shows that *M* and *CC* values decrease with the distance between the nodes. It can be seen that the mutual inductance in an *L*-bend is negligible when compared to the mutual inductance arising from the neighboring lines and the ground plane as seen from table 2.2. However, the coupling capacitance in an *L*-bend has a small effect when the distance between the nodes of the *L*-bend is less than 2-3μm, as the coupling capacitance is inversely proportional to the distance between the nodes. Thus, for interconnect lengths exceeding a few micrometers as in the case of intermediate and global interconnects whose length far exceeds hundreds of micrometers, the effect of self coupling in an *L*-bend can be ignored when compared to the coupling from the ground and neighboring lines.

Table 2.3: Comparision of relative percentage change in the values of M and CC

Length between Segments (mm)	Diagonal Distance (mm)	M (pH)	% change in M	CC (fF)	% change in CC
0.30	0.2121	44.81	-	0.667	-
0.45	0.3345	65.97	47.2	0.402	39.73
0.60	0.474	86.26	30.75	0.273	32.08
0.75	0.618	106.61	23.59	0.204	25.27
0.90	0.7635	127.07	19.19	0.162	20.58
1.05	0.912	147.5	16.07	0.132	18.51
1.20	1.0605	168.11	13.97	0.112	15.15
1.35	1.2095	188.73	12.26	0.097	13.39

2.4.4 Generalized State Space Model of a T section

Figure 2.12(d) shows 3D view of the **T** interconnect structure and the generalized equivalent RLGC network is given in figure 2.20. The horizontal, upper and lower wings of the interconnect are named as h, u and d respectively. Resistance, inductance, conductance and capacitances of the horizontal, upper and lower wings are represented by the corresponding subscripts. The coupling capacitance and mutual inductance between i^{th} segment of the horizontal wing to the j^{th} and k^{th} segment in the upper and lower wings are represented by CC_{iuj}, CC_{idk}, M_{iuj} and M_{idk} respectively. State variables associated with the capacitors (V_{h1} to V_{hn}, V_{u1} to V_{un} and V_{d1} to V_{dn}) and inductors (I_{h1} to I_{hn}, I_{u1} to I_{un} and I_{d1} to I_{dn}) in the left and right wing are shown in figure 2.20. Generalized state matrices are derived and expressed as follows.

$$\mathbf{E_{Tsect}} = \begin{bmatrix} \mathbf{E_{T11}} & \mathbf{E_{T12}} & \mathbf{E_{T13}} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{E_{T22}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{E_{T33}} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{E_{T44}} & \mathbf{E_{T45}} & \mathbf{E_{T46}} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{E_{T54}} & \mathbf{E_{T55}} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{E_{T64}} & \mathbf{0} & \mathbf{E_{T66}} \end{bmatrix} \tag{2.30}$$

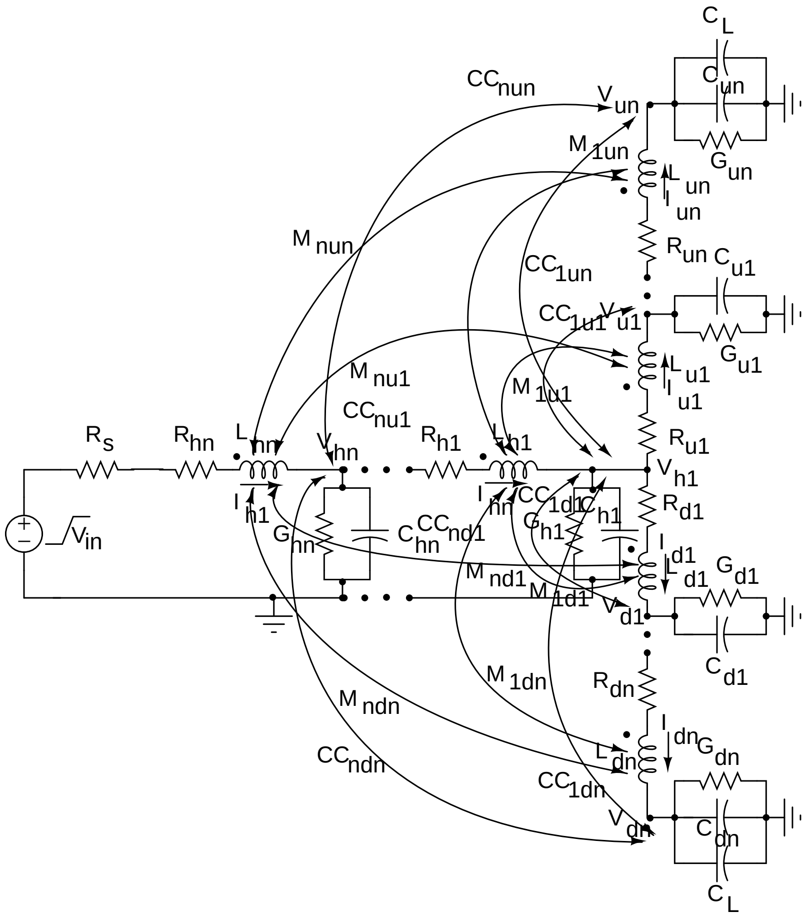


Figure 2.20: Generalized RLGC model of the **T**-section

$$\mathbf{A_{Tsect}} = \begin{bmatrix} \mathbf{A_{T11}} & \mathbf{0} & \mathbf{0} & \mathbf{A_{T14}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{A_{T22}} & \mathbf{0} & \mathbf{A_{T24}} & \mathbf{A_{T25}} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{A_{T33}} & \mathbf{A_{T34}} & \mathbf{0} & \mathbf{A_{T36}} \\ \mathbf{A_{T41}} & \mathbf{A_{T42}} & \mathbf{A_{T43}} & \mathbf{A_{T44}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{A_{T52}} & \mathbf{0} & \mathbf{0} & \mathbf{A_{T55}} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{A_{T63}} & \mathbf{0} & \mathbf{0} & \mathbf{A_{T66}} \end{bmatrix} \tag{2.31}$$

For the convenience to derive state space matrices, equal number of RLGC segments have been considered in the horizontal, upper and lower wings of **T** interconnect structure (figure 2.20). In equations (2.30) and (2.31), every element is a matrix whose size depends on the number of capacitive (or inductive) state variables present in the horizontal (or upper or lower) wing of the RLGC interconnect network. The generalized matrix structures of the elements in equations (2.30) and (2.31) are given below.

$$\mathbf{E_{T11}} = \mathbf{E_{T22}} = \mathbf{E_{T33}} = \begin{bmatrix} L_{h1/u1/d1} & 0 & \cdots & 0 \\ 0 & L_{h2/u2/d2} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & L_{hn/un/dn} \end{bmatrix}$$

$$\mathbf{E_{T12}} = \begin{bmatrix} M_{1u1} & M_{1u2} & \cdots & M_{1un} \\ M_{2u1} & M_{2u2} & \cdots & M_{2un} \\ \vdots & \vdots & \vdots & \vdots \\ M_{nu1} & M_{nu2} & \cdots & M_{nun} \end{bmatrix}$$

$$\mathbf{E_{T22}} = \begin{bmatrix} L_{u1} & 0 & \cdots & 0 \\ 0 & L_{u2} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & L_{un} \end{bmatrix}$$

$$\mathbf{E_{T13}} = \begin{bmatrix} M_{1d1} & M_{1d2} & \cdots & M_{1dn} \\ M_{2d1} & M_{2d2} & \cdots & M_{2dn} \\ \vdots & \vdots & \vdots & \vdots \\ M_{nd1} & M_{nd2} & \cdots & M_{ndn} \end{bmatrix}$$

$$\mathbf{E_{T44}} = \begin{bmatrix} A & 0 & \cdots & 0 \\ 0 & B & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & H \end{bmatrix}$$

The diagonal elements A to H of $\mathbf{E_{T44}}$ in general are defined as $C_{hi} + CC_{iu1} + \ldots +$

$CC_{iun} + CC_{id1} + \ldots + CC_{idn}$.

$$\mathbf{E_{T33}} = \begin{bmatrix} L_{d1} & 0 & \cdots & 0 \\ 0 & L_{d2} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & L_{dn} \end{bmatrix}$$

$$\mathbf{E_{T45}} = \mathbf{E_{T54}} = \begin{bmatrix} -CC_{1u1} & -CC_{1u2} & \cdots & -CC_{1un} \\ -CC_{2u1} & -CC_{2u2} & \cdots & -CC_{2un} \\ \vdots & \vdots & \vdots & \vdots \\ -CC_{nu1} & -CC_{nu2} & \cdots & -CC_{nun} \end{bmatrix}$$

$$\mathbf{E_{T46}} = \mathbf{E_{T64}} = \begin{bmatrix} -CC_{1d1} & -CC_{1d2} & \cdots & -CC_{1dn} \\ -CC_{2d1} & -CC_{2d2} & \cdots & -CC_{2dn} \\ \vdots & \vdots & \vdots & \vdots \\ -CC_{nd1} & -CC_{nd2} & \cdots & -CC_{ndn} \end{bmatrix}$$

$$\mathbf{E_{T55}} = \begin{bmatrix} I & 0 & \cdots & 0 \\ 0 & J & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & P \end{bmatrix}$$

$$\mathbf{E_{T66}} = \begin{bmatrix} R & 0 & \cdots & 0 \\ 0 & S & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & Y \end{bmatrix}$$

In general, diagonal elements I to P in $\mathbf{E_{T55}}$ and R to Y in $\mathbf{E_{T66}}$ are defined as $C_{ui} +$

$CC_{1ui} + \ldots + CC_{nui}$ and $C_{di} + CC_{1di} + \ldots + CC_{ndi}$ respectively.

$$\mathbf{A_{T11}} = \mathbf{A_{T22}} = \mathbf{A_{T33}} = \begin{bmatrix} -R_{h1/u1/d1} & 0 & \cdots & 0 \\ 0 & -R_{h2/u2/d2} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & -R_{hn/un/dn} \end{bmatrix}$$

$$\mathbf{A_{T14}} = \mathbf{A_{T25}} = \mathbf{A_{T36}} = \begin{bmatrix} -1 & 0 & \cdots & 0 & 0 \\ 1 & -1 & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \ddots & \vdots \\ 0 & 0 & \cdots & 1 & -1 \end{bmatrix}$$

$$\mathbf{A_{T24}} = \mathbf{A_{T34}} = \begin{bmatrix} 1 & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & 0 \\ 0 & 0 & \cdots & 0 \end{bmatrix}$$

$$\mathbf{A_{T41}} = \mathbf{A_{T52}} = \mathbf{A_{T63}} = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 \\ -1 & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \ddots & \vdots \\ 0 & 0 & \cdots & -1 & 1 \end{bmatrix}$$

$$\mathbf{A_{T43}} = \mathbf{A_{T44}} = \begin{bmatrix} -1 & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & 0 \\ 0 & 0 & \cdots & 0 \end{bmatrix}$$

$$\mathbf{A_{T44}} = \mathbf{A_{T55}} = \mathbf{A_{T66}} = \begin{bmatrix} -G_{h1/u1/d1} & 0 & \cdots & 0 \\ 0 & -G_{h2/u2/d2} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & -G_{hn/un/dn} \end{bmatrix}$$

To validate the model, a step signal of voltage 1.8 V at the free end of the horizontal

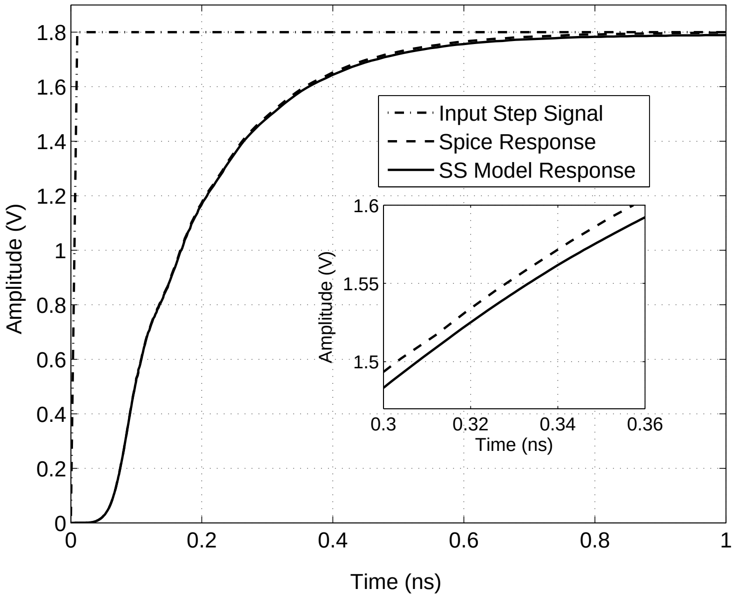


Figure 2.21: Comparison of state space model and SPICE responses of the T-section

wing of the **T** interconnect structure is applied and the responses at the other end of the upper or lower wing are measured. The SPICE and state space responses are plotted in figure 2.21 and found to be closely matching.

2.4.4.1 *M* and *CC* Values between the Nodes of the *T* Structure

In the generalized RLGC model of the **T**-structure in figure 2.20, mutual inductances (*M*) and coupling capacitances (*CC*) are taken into account from each node of the horizontal wing to all the nodes of the upper and lower wings. Computing the values of *M* and *CC* is similar to the **L** interconnect structure given in section 2.4.3.1. In this case also, it is found that the effects of *M* and *CC* are marginal beyond the first nodes on either side of the T-section.

2.5 Modeling the Interconnect with arbitrary Manhattan Shape

Intermediate and Global interconnects have longer lengths and large wire pitch when compared to local interconnects. Consequently, delay and coupling effects associated with these interconnects are significantly larger than that of local interconnects. In an IC, intermediate and global interconnects usually used for routing the power signals, ground lines, clock networks and signal distribution between the functional blocks. These interconnect lines may have Manhattan geometry shapes such as $\sqcup$, $\sqsubset$, $\urcorner\!\llcorner$ or $\top$.

Using the models proposed in section 2.4, interconnects of Manhattan shape can be modeled by segmenting and classifying each segment into one of the above four categories. For example, a tuning fork shaped interconnect can be segmented into two **L**-sections at the bending portion, one **T**-section in the branching portion and the rest as one set of parallel interconnect lines or two distinct single lines depending upon their relative separation.

To illustrate this, consider the network shown in figure 2.22. This structure is modeled as a combination of single, **T**-section, **L**-sections and coupled lines in cascade form with a line length of 2.7 *mm* between ‘S’ and ‘F’ and a line length of 3.7 *mm* between ‘S’ and ‘G’. Lengths of the different sections of the tuning fork shaped interconnect structure considered is given below. A source is connected at the end ‘S’ of the interconnect structure and the response is observed at ‘F’ and ‘G’ ends. The overall model of this generic interconnect is obtained by a combination of single, coupled, **L** and **T**-section models.

1. To the left of AA' (horizontal section) and between BB' to EE' (vertical section), single line models are used.
2. **T** model is used for the region enclosed by the rectangle $BB'C'C$.
3. **L** section models are used for the segments CC' to $C'D$ and EE' to $E'D'$.
4. Coupled line model is used to the right of DD'.

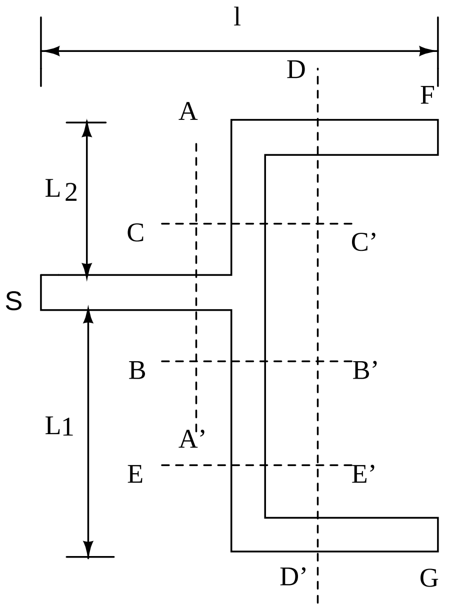


Figure 2.22: Top view of a generic interconnect line

2.5.0.2 Cascading Different Interconnect Models

Upper part in figure 2.22 is represented as the cascaded sections of different models as shown in figure 2.23. Final output is taken at *DF* of the coupled interconnect which corresponds to the output at point *F* in figure 2.22. The state matrices for different interconnect structures in section 2.4 are modified so that these models can be connected in cascade to determine the final output.

The modification in the modeling is explained by considering the horizontal section of 1 *mm* length interconnect (to the left of AA') in figure 2.22. Single interconnect line is represented by 6 RLGC segments as shown in figure 2.24. Equation (2.22) is expanded and written as shown in equations (2.32) and (2.33). The **D** matrix is a null matrix as there is no feed forward path from input to output.

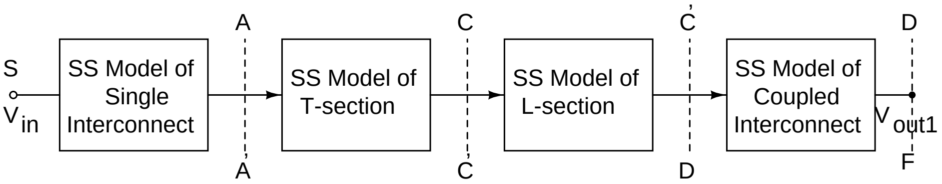


Figure 2.23: Modeling the upper part of the generic interconnect line by cascading different interconnect sections

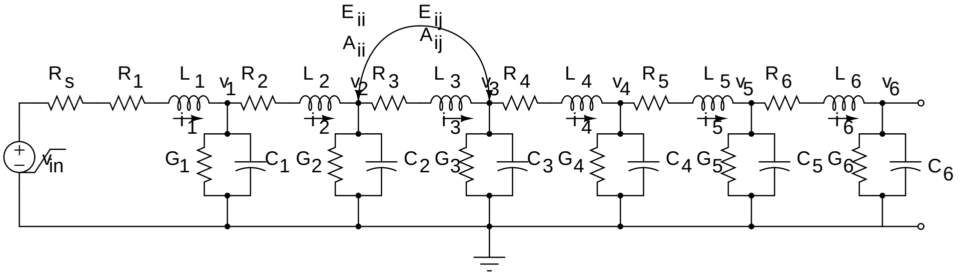


Figure 2.24: Single interconnect represented by 6 RLGC segments

$$\begin{bmatrix} \mathbf{E_{11}} & \mathbf{E_{12}} & \mathbf{E_{13}} & \mathbf{E_{14}} & \mathbf{E_{15}} & \mathbf{E_{16}} \\ \mathbf{E_{21}} & \mathbf{E_{22}} & \mathbf{E_{23}} & \mathbf{E_{24}} & \mathbf{E_{25}} & \mathbf{E_{26}} \\ \mathbf{E_{31}} & \mathbf{E_{32}} & \mathbf{E_{33}} & \mathbf{E_{34}} & \mathbf{E_{35}} & \mathbf{E_{36}} \\ \mathbf{E_{41}} & \mathbf{E_{42}} & \mathbf{E_{43}} & \mathbf{E_{44}} & \mathbf{E_{45}} & \mathbf{E_{46}} \\ \mathbf{E_{51}} & \mathbf{E_{52}} & \mathbf{E_{53}} & \mathbf{E_{54}} & \mathbf{E_{55}} & \mathbf{E_{56}} \\ \mathbf{E_{61}} & \mathbf{E_{62}} & \mathbf{E_{63}} & \mathbf{E_{64}} & \mathbf{E_{65}} & \mathbf{E_{66}} \end{bmatrix} \begin{bmatrix} \mathbf{\dot{x}_1} \\ \mathbf{\dot{x}_2} \\ \mathbf{\dot{x}_3} \\ \mathbf{\dot{x}_4} \\ \mathbf{\dot{x}_5} \\ \mathbf{\dot{x}_6} \end{bmatrix} = \begin{bmatrix} \mathbf{A_{d11}} & \mathbf{A_{d12}} & \mathbf{A_{d13}} & \mathbf{A_{d14}} & \mathbf{A_{d15}} & \mathbf{A_{d16}} \\ \mathbf{A_{d21}} & \mathbf{A_{d22}} & \mathbf{A_{d23}} & \mathbf{A_{d24}} & \mathbf{A_{d25}} & \mathbf{A_{d26}} \\ \mathbf{A_{d31}} & \mathbf{A_{d32}} & \mathbf{A_{d33}} & \mathbf{A_{d34}} & \mathbf{A_{d35}} & \mathbf{A_{d36}} \\ \mathbf{A_{d41}} & \mathbf{A_{d42}} & \mathbf{A_{d43}} & \mathbf{A_{d44}} & \mathbf{A_{d45}} & \mathbf{A_{d46}} \\ \mathbf{A_{d51}} & \mathbf{A_{d52}} & \mathbf{A_{d53}} & \mathbf{A_{d54}} & \mathbf{A_{d55}} & \mathbf{A_{d56}} \\ \mathbf{A_{d61}} & \mathbf{A_{d62}} & \mathbf{A_{d63}} & \mathbf{A_{d64}} & \mathbf{A_{d65}} & \mathbf{A_{d66}} \end{bmatrix} \begin{bmatrix} \mathbf{x_1} \\ \mathbf{x_2} \\ \mathbf{x_3} \\ \mathbf{x_4} \\ \mathbf{x_5} \\ \mathbf{x_6} \end{bmatrix} + \begin{bmatrix} \mathbf{B_{d1}} \\ \mathbf{B_{d2}} \\ \mathbf{B_{d3}} \\ \mathbf{B_{d4}} \\ \mathbf{B_{d5}} \\ \mathbf{B_{d6}} \end{bmatrix} \begin{bmatrix} \mathbf{u} \end{bmatrix} \tag{2.32}$$

$$\begin{bmatrix} \mathbf{y} \end{bmatrix} = \begin{bmatrix} \mathbf{C_1} & \mathbf{C_2} & \mathbf{C_3} & \mathbf{C_4} & \mathbf{C_5} & \mathbf{C_6} \end{bmatrix} \begin{bmatrix} \mathbf{x_1} \\ \mathbf{x_2} \\ \mathbf{x_3} \\ \mathbf{x_4} \\ \mathbf{x_5} \\ \mathbf{x_6} \end{bmatrix} \tag{2.33}$$

where the input variables ($\mathbf{x_i}$ and $\mathbf{u}$) and output variable ($\mathbf{y}$) are defined as

$$\mathbf{x_1} = \begin{bmatrix} i_1 & v_1 \end{bmatrix}^T$$

$$\mathbf{x_2} = \begin{bmatrix} i_2 & v_2 \end{bmatrix}^T$$

$$\mathbf{x_3} = \begin{bmatrix} i_3 & v_3 \end{bmatrix}^T$$

$$\mathbf{x_4} = \begin{bmatrix} i_4 & v_4 \end{bmatrix}^T$$

$$\mathbf{x_5} = \begin{bmatrix} i_5 & v_5 \end{bmatrix}^T$$

$$\mathbf{x_6} = \begin{bmatrix} i_6 & v_6 \end{bmatrix}^T$$

$$\mathbf{u} = \begin{bmatrix} v_{in} \end{bmatrix}$$

$$\mathbf{y} = \begin{bmatrix} v_6 \end{bmatrix}$$

In equation (2.32), $\mathbf{E_{ii}}$ and $\mathbf{E_{ij}}$ represents the capacitive and inductive coupling effects associated with the node i and between i and j respectively. Similarly $\mathbf{A_{dii}}$ and $\mathbf{A_{dij}}$ indicates the resistance and conductance connected to node i and between i and j respectively. The dimensions of the sub matrices in equation (2.32) are as as follows.

dim$\left[\mathbf{E_{ij}}\,(.)\right]$=2×2
dim$\left[\mathbf{A_{dij}}\,(.)\right]$=2×2
dim$[\mathbf{B_{di}}\,(.)]$=2×1 and
dim$[\mathbf{C_{i}}\,(.)]$=1×2.

The output is taken at node v_6 of figure 2.24. Hence,

$$\mathbf{C_i} = \begin{bmatrix} \mathbf{0} \end{bmatrix}_{1\times 2}, \qquad i = 1,2,3,4,5$$

$$\mathbf{C_6} = \begin{bmatrix} 0 & 1 \end{bmatrix}$$

By noting that the 6 segments in figure 2.24 are cascaded one after another, the elements of equations (2.32) and (2.33) are rearranged to correctly compute the output. The modified equations are given by,

$$\begin{bmatrix} \mathbf{E_{11}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{E_{22}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{E_{33}} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{E_{44}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{E_{55}} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{\dot{x}_1} \\ \mathbf{\dot{x}_2} \\ \mathbf{\dot{x}_3} \\ \mathbf{\dot{x}_4} \\ \mathbf{\dot{x}_5} \\ \mathbf{\dot{x}_6} \end{bmatrix} = \begin{bmatrix} \mathbf{A_{d11}} & \mathbf{A_{d12}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{A_{d21}} & \mathbf{A_{d22}} & \mathbf{A_{d23}} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{A_{d32}} & \mathbf{A_{d33}} & \mathbf{A_{d34}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{A_{d43}} & \mathbf{A_{d44}} & \mathbf{A_{d45}} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{d54}} & \mathbf{A_{d55}} & \mathbf{A_{d56}} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{d65}} & \mathbf{A_{d66}} \end{bmatrix} \begin{bmatrix} \mathbf{x_1} \\ \mathbf{x_2} \\ \mathbf{x_3} \\ \mathbf{x_4} \\ \mathbf{x_5} \\ \mathbf{x_6} \end{bmatrix} + \begin{bmatrix} \mathbf{B_{d1}} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} \begin{bmatrix} V_{in} \end{bmatrix} \tag{2.34}$$

$$\begin{bmatrix} y \end{bmatrix} = \begin{bmatrix} \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{C_6} \end{bmatrix} \begin{bmatrix} \mathbf{x_1} \\ \mathbf{x_2} \\ \mathbf{x_3} \\ \mathbf{x_4} \\ \mathbf{x_5} \\ \mathbf{x_6} \end{bmatrix} \tag{2.35}$$

The submatrices in equations (2.34) and (2.35) are defied as below.

$$\mathbf{E_{ii}} = \left[\begin{array}{c|cc} & i_i & v_i \\ \hline i_i & L_i & 0 \\ v_i & 0 & C_i \end{array}\right]$$

$$\mathbf{A_{dii}} = \left[\begin{array}{c|cc} & i_i & v_i \\ \hline i_i & -R_i & -1 \\ v_i & 1 & -G \end{array}\right]$$

$$\mathbf{A_{dij}} = \left[\begin{array}{c|cc} & i_j & v_j \\ \hline i_i & 0 & 0 \\ v_i & -1 & 0 \end{array}\right]$$

$$\mathbf{A_{dji}} = \left[\begin{array}{c|cc} & i_i & v_i \\ \hline i_j & 0 & 1 \\ v_i & 0 & 0 \end{array}\right]$$

$$\mathbf{C_6} = \begin{bmatrix} 0 & 1 \end{bmatrix}$$

$$\mathbf{B_{d1}} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

In the above sub-matrices, i_i and v_i denotes the current and voltage associated with i^{th} node. Similarly, i_j and v_j indicates the current and voltage associated with j^{th} node. State space matrices are defined in a similar manner for Coupled, **L** and **T**-section interconnects. The cascading connection of single line interconnect and **T**-section is defined as,

$$\mathbf{A_{dkl}} = \left[\begin{array}{c|cc} & i_l & v_l \\ \hline i_k & 0 & 0 \\ v_k & -1 & 0 \end{array}\right]$$

$$\mathbf{A_{dlk}} = \left[\begin{array}{c|cc} & i_k & v_k \\ \hline i_l & 0 & 1 \\ v_l & 0 & 0 \end{array}\right]$$

where $\mathbf{A_{dkl}}$ sub-matrix represents the relationship between the state variables of the last node k of the single line interconnect and the first node l of the **T**-section model. Similarly sub-matrices are defined for joining the upper **T** - **L** sections and **L** - Coupled interconnect sections. In both the cases, the sub-matrices are defined similar to $\mathbf{A_{dkl}}$ and $\mathbf{A_{dlk}}$.

To validate the model, a step signal of voltage 1.8 V is applied at the free end of the horizontal wing (point S in figure 2.22) of the single line interconnect structure and the response is measured at point F. The SPICE and state space responses are plotted in figure 2.25 and found to be closely matching.

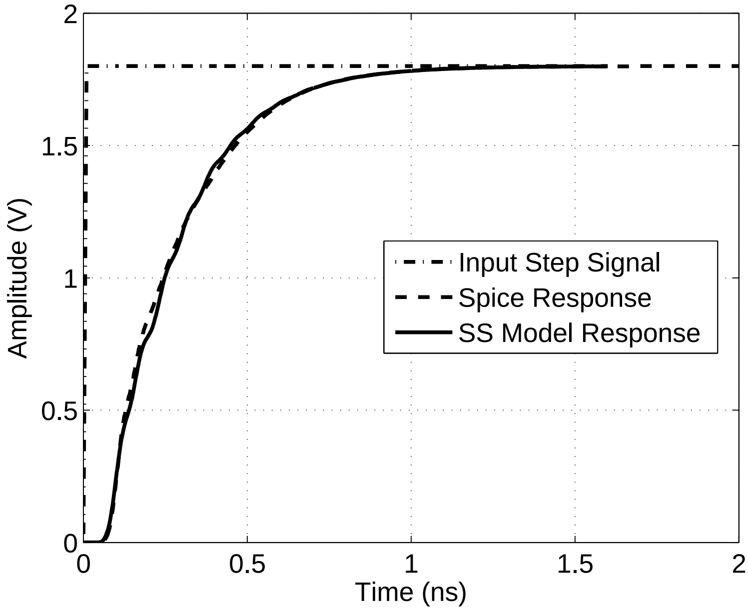


Figure 2.25: Comparison of state space model and SPICE responses at F in 2.22

2.5.1 Interconnect Metrics for Different Technology Nodes

State space matrices for different proposed interconnect models (single, coupled, **L** and **T**) are implemented using Matlab functions. Interconnect metrics like 50% time delay (t_d), rise time (t_r) and cut-off frequency (f_c) for different technology nodes are calculated using the interconnect parasitics given in table 2.2. Table 2.4 shows the measured interconnect metrics for the same using the proposed models for the interconnect length of 2.5 *mm*. Figure 2.26 to 2.30 shows the frequency response of the proposed models for 65nm technology parameters.

Table 2.4: Interconnect metrics for the proposed models at different technology nodes

Technology	Proposed Models	t_d (ps)	t_r (ps)	f_c (GHz)
180 *nm*	Single	75	49	35.48
	Coupled	103	146	17.78
	L-section	101	174	14.45
	T-section	110	149	15.275
130 *nm*	Single	81	87	25.12
	Coupled	113	176	14.79
	L-section	110	216	10.96
	T-section	121	181	11.48
90 *nm*	Single	92	140	14.79
	Coupled	131	319	7.94
	L-section	123	247	8.7498
	T-section	133	276	7.834
65 *nm*	Single	98	161	13.18
	Coupled	131	283	8.51
	L-section	132	273	7.94
	T-section	138	299	7.24
45 *nm*	Single	446	876	1.814
	Coupled	730	1815	1
	L-section	463	1257	1.722
	T-section	648	858	1.148
32 *nm*	Single	787	792	1
	Coupled	1308	1683	0.552
	L-section	801	1600	0.928
	T-section	1150	1756	0.631

From table 2.4, it can be seen that time delay and rise time through the interconnect increases as the technology node decreases. The cut-off frequency of the coupled, **L** and **T**-section for the same technology node is nearly half of the single interconnect line. The effect of mutual inductance and coupling capacitance increases the signal

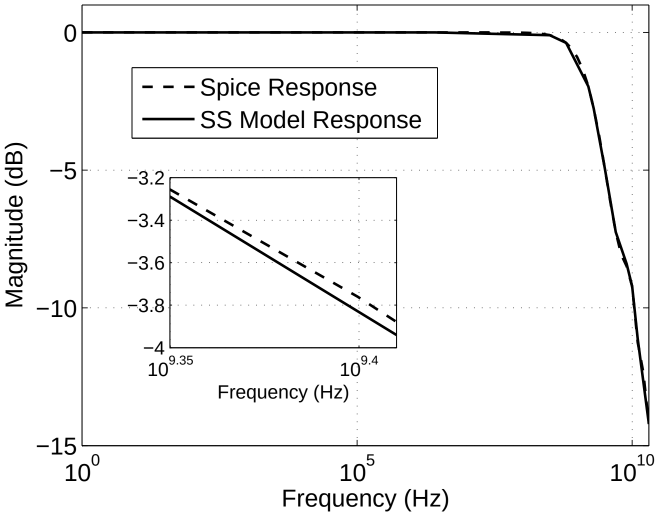


Figure 2.26: Frequency response of the single interconnect line

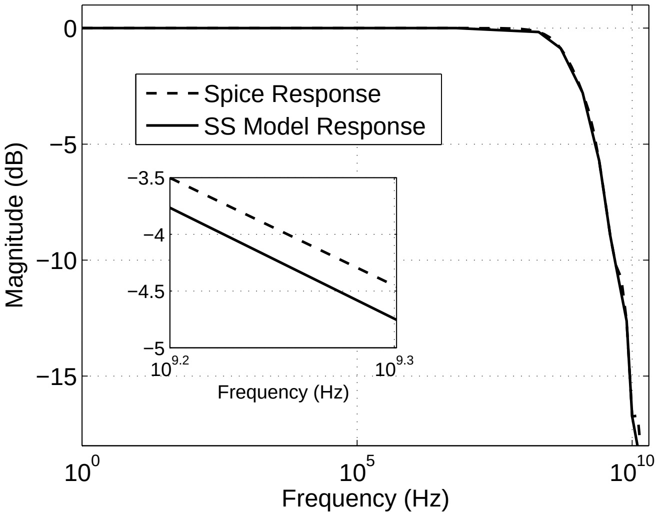


Figure 2.27: Frequency response of the Coupled interconnect (aggressor response)

propagation delay and decreases the cutoff frequency range.

Generally, unlike in PCB's, interconnects in an IC are drawn as parallel lines in a given layer and a L-section or a T-section is formed by connecting the lines of different layers (3-D structure) using a via. Thus, a L- or a T-section of wire comprises interconnects of two layers, possibly with different metrics (width, thickness, spacing etc), and the via with its parasitics. Thus, in the delay estimation model, the state space matrix elements will have different values depending upon the layer and the via parameters.

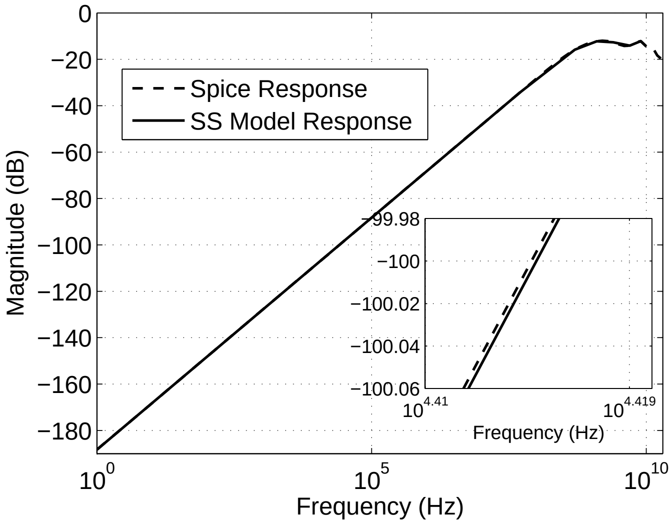


Figure 2.28: Frequency response of the Coupled interconnect (victim response)

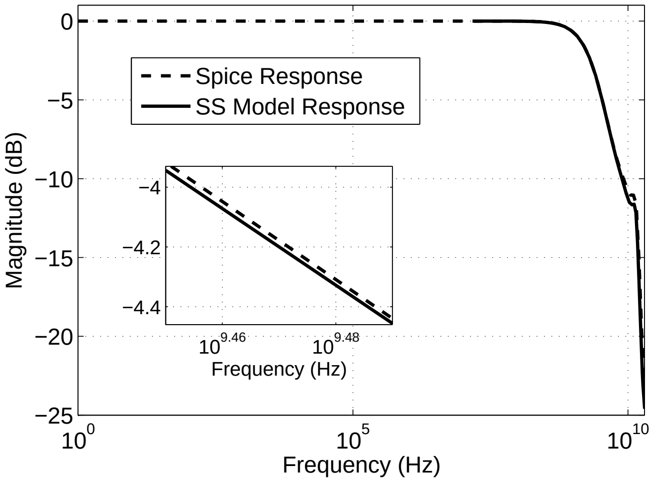


Figure 2.29: Frequency response of the L-segment

Therefore in such cases, while computing the signal delays using state space approach, matrix elements have to be chosen appropriately to obtain correct delay values.

2.6 Conclusions

State space approach is used to model single, coupled, **L** and **T** type interconnect lines. Model for the parallel coupled interconnects is derived by including the mutual inductance and coupling capacitances between the coupled lines. State space model of the

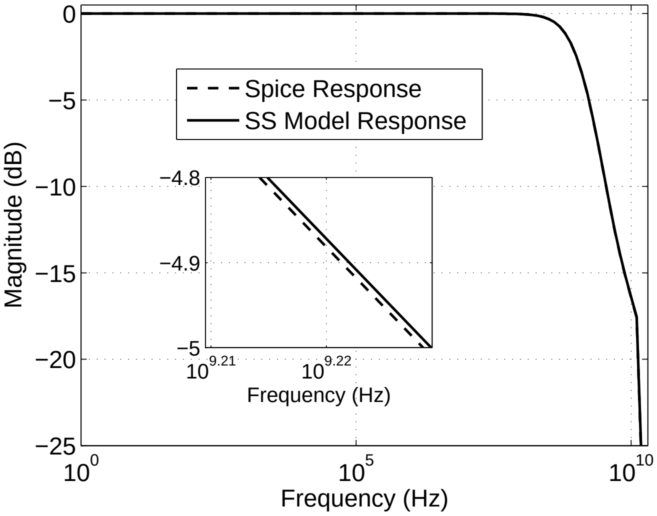


Figure 2.30: Frequency response of the T-segment

two-coupled interconnects can easily be extended to multi-coupled interconnects using the modular matrix structure. Models for the **L** and **T** type of interconnects are derived by considering the coupling effects between the branched segments of the same line. Each model response is compared with the SPICE simulation and it is found that the model responses are closely matching with the SPICE responses.

Using the proposed models, interconnects with any Manhattan geometry shapes, such as ⊔, ⊏, ⅂ or ⊤ can be modeled. This is demonstrated by modeling a tuning fork shaped interconnect structure into two **L**-sections at the bending portion, one **T**-section in the branching portion and the rest as one set of parallel interconnect lines or two distinct single lines depending upon their relative separation.

Interconnect metrics are calculated from the models for 180 *nm*, 130 *nm*, 90 *nm*, 65 *nm*, 45 *nm* and 32 *nm* technology nodes. The models are valid for wide range of operating frequencies. Simulation results indicate the dominance of interconnect delay with technology scaling. The numerical computations confirm that the proposed modeling method enables to evaluate accurately the transient signal parameters like rise/fall-times and propagation delay in very less computation time. For this reason, this analytical modeling method is potentially interesting for the analysis of the signal integrity in high-speed complex interconnection networks.

The computation complexity of the State-space closed forms of the distributed RLGC line interconnect is $O(n)$ (Wang and Wang, 2010). Whereas, simulation tools such as SPICE no doubt gives accurate results albeit with a computational complexity of $O(n^2)$ for 2D RC-extraction with n nodes. However, extracting complex 3D structures taking into account the inductive effects would lead to very large equivalent circuits and the complexity would significantly increase leading to increased simulation time. The approach presented in thesis would permit us to reduce the order of the equivalent circuit and considerably reduce the simulation time even for large networks.

Proposed models are modular in nature and can be extended to any interconnect length. These models can be used to estimate the metrics of nonuniform interconnect structures. Estimating interconnect metrics such as delay, rise time, fall time, cutoff frequency etc. for such models would be difficult using SPICE.

CHAPTER 3

Crosstalk Estimation and Model Order Reduction

3.1 Crosstalk Estimation in Coupled Interconnects using State Space Approach

3.1.1 Introduction

In integrated circuit design, crosstalk normally refers to a signal affecting another nearby signal. Crosstalk is the coupling of energy to the neighboring line(s) when electromagnetic fields from nearby structures interact. The line which is affecting its neighbor is termed as aggressor while the affected neighbor is termed as victim line. Usually the coupling is capacitive, and to the nearest neighbor, but other forms of coupling and effects on signal farther away are also important. In a complicated multi-layered interconnect system, signal coupling strongly affects the circuit performance. Coupled noise causes undesired effects such as glitches, overshoots, undershoots and even functional failures. The magnitude of these effects depend on the switching combinations of the input signals and the proximity of the aggressor to the victim line.

Several solutions are proposed to reduce the crosstalk-induced effects at different stages of IC design . Net ordering, repeater insertion and wire shielding are some of the widely used solutions employed at the physical level to reduce crosstalk noise voltages ((Zhang and Friedman, 2006), (Kaushik *et al.*, 2011)).

The aforementioned schemes do not necessarily guarantee an acceptable interconnect performance at the chip level. Crosstalk noise in the coupled interconnects cannot be completely suppressed but accurate and proper estimation of the crosstalk noise voltage will help the designers while designing the layout of an IC chip. The designers can concentrate on the locations where the probability of appearing coupled noise is maximum. Depending on the application of the ICs and complexity level, some solutions can be adopted to reduce the coupled noise voltages to its minimum level while designing the layout. This will help to improve the performance and reliability of closely placed interconnect layers in an IC chip to a great extent.

Sakurai derived the expression to estimate the coupled noise voltage in the victim line of the distributed RC network (Sakurai, 1993) and presented its step response as a power series. Since the series is too complicated to analytically solve, he approximated the circuit to its first-order and extended the expression for the output voltage of two-coupled lines. Based on this, closed form expression is derived to estimate the crosstalk noise in the victim line. In (Eo *et al.*, 2000), crosstalk estimation model for coupled CMOS circuits is derived based on realistic assumptions. In this work, CMOS circuits are modeled as resistance at the driving port and capacitance at the load port. Compact expression for the estimation of crosstalk in distributed RLC lines with capacitive load is presented in (Venkatesan *et al.*, 2003*b*). In this paper, while modeling, it is considered that two signal interconnects are flanked by shielding power/ground lines and sandwiched between the ground planes. It is shown in (Zhang and Friedman, 2004) that the accuracy of crosstalk estimation can be improved by using a decoupling technique.

In DSM regime, on-chip inductive effects are rising due to increasing clock speeds, decreasing interconnect lengths and signal rise times. In intermediate/global interconnects, inductive effects are severe when compared to other parasitic effects due to the lower resistance of these lines and this fact is validated by considering an analytical model for inductive crosstalk in (Ravindra and Srinivas, 2007).

Distributed RLC based analytical model for the estimation of the peak crosstalk noise voltage under worst noise condition is proposed in (Kadim and Coulibaly, 2006). In (Palit *et al.*, 2005), ABCD modeling approach is used to model the crosstalk coupling noise on the victim interconnect due to single or multiple aggressors. Different expressions to calculate the crosstalk noise voltages for in-phase and out-of-phase switching combination of the input signals in coupled interconnects using distributed RLC model are derived in (Kaushik *et al.*, 2011). In another approach, distributed decoupled victim wire model is developed by considering into account all possible sources of coupling noise (mutual capacitance and mutual inductance between the two adjacent aggressor-victim lines) (Palit *et al.*, 2009). These parameters are decoupled and their effect is considered only on the victim line as a function of aggressors and victims switching directions. The advantage of this model is that by using this decoupled model, it is possible to simulate and analyze the crosstalk glitch and delay effects on the victim interconnect for various combinations of input signals. The literature presented here on crosstalk noise is in no way exhaustive and a listing of the current literature would be beyond the scope of this thesis.

So far, crosstalk noise estimation is done based on lumped RC/distributed RC/distributed RLC network model of the interconnects. In most of the published works for coupled interconnects, crosstalk estimation models change with the input switching combinations. Also, expressions to determine coupled noise voltages can not be extend to more than two-coupled interconnects. Hence, estimating the crosstalk noise in the victim lines of the multi-coupled interconnects is difficult. Further, in all these models it is observed that the estimated crosstalk noise voltage differs with the SPICE response by an average of 8% or more.

In this work, firstly, the crosstalk noise estimation is done using the RLGC network model which is more accurate than previously used lumped and distributed RC / RLC models. Secondly, the noise estimation is extended from two coupled lines to multi-coupled lines. This takes into account the noise induced in the victim line by the aggressors that are not in the immediate neighborhood. Further, the noise estimation is done using state space approach. Generalized state space matrices are derived in section 2.4.2 for the distributed RLGC network of the two coupled interconnects considering n segments. Input matrix (B), output matrix (C) along with E and A matrices are used to estimate the crosstalk noise voltages in the victim lines of the coupled interconnects. The state space matrices so obtained are modular in nature and can be easily extended to multi-coupled interconnect lines to estimate the coupled noise in the victim lines. This is illustrated by estimating the coupled noise voltages in the victim lines of the five coupled interconnects.

3.1.2 Crosstalk Noise Voltage Estimation in the Victim Line of Two-Coupled Interconnects

Generalized state space matrices of E and A for the two-coupled interconnect lines are given in equations (2.26) and (2.27). These matrices are used along with B and C matrices to find the crosstalk noise in the victim lines of the coupled interconnects. In order to estimate the coupled noise, consider a representative coupled line with 4 RLGC sections in each line as shown in figure 3.1. State space matrices E, A, B and C for the network in figure 3.1 are in modular form. Dimensions of these matrices are 16×16 (for $n \times n$, n is given by: 2 state variables per section × number of sections per line × number of coupled lines), 16×16, 16×2 ($n \times p$ where p is the number of inputs, in this case $p = 2$) and 2×16 ($q \times n$ where q is the number of output variables, in this case $q = 2$) respectively.

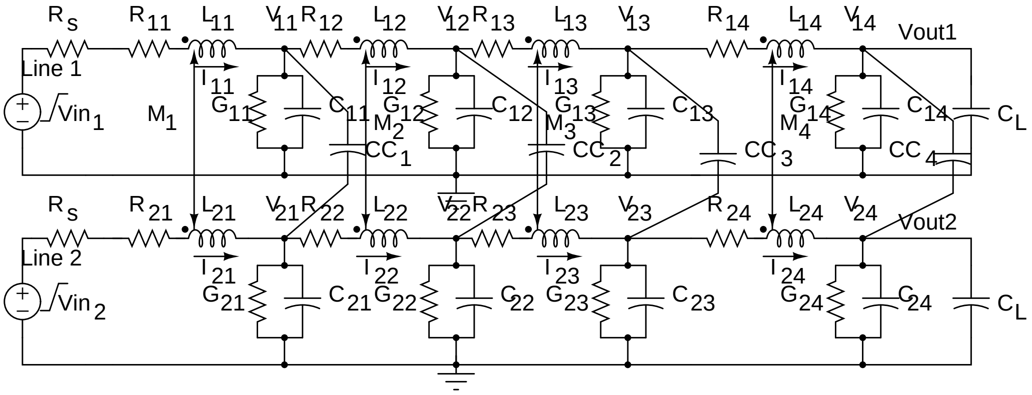


Figure 3.1: Two-coupled interconnects with 4 RLGC segments each

To find the coupled noise voltage in Line 2 (at node V_{out2} of the victim line), when an input signal is applied to Line 1 (aggressor line), matrices B and C shown in equations (3.1) and (3.2) are used. In equation (3.2), elements of 1^{st} to 8^{th} column and 9^{th} to 16^{th} column in the first and second row represent the loop currents and the node voltages in Line 1 and Line 2 respectively of the network shown in figure 3.1. Loop currents or node voltages are computed by making the corresponding entry as 1 in equation (3.2).

For example, to compute the coupled noise voltage in Line 2 at node V_{out2}, 16^{th} column entry in 2^{nd} row of equation (3.2) is made 1.

$$\mathbf{B_{input\_2coup}} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{3.1}$$

$$\mathbf{C_{crosstalk\_est\_2coup}} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{3.2}$$

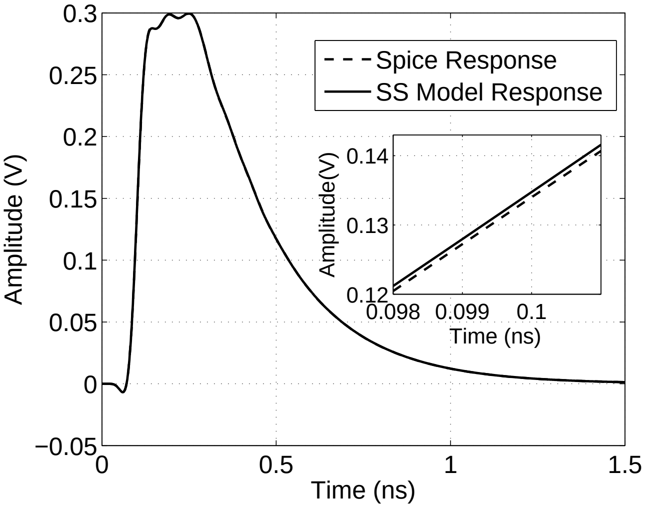


Figure 3.2: Comparison of state space model and SPICE responses of the coupled noise in the victim line of the two-coupled interconnects

To validate the crosstalk estimation model, a step signal of 1.8 V is applied to one end of the Line 1. The crosstalk voltage is measured at node V_{out2} of Line 2 (figure 3.1). The model and SPICE responses are plotted in figure 3.2 and found to be closely matching.

3.1.3 Crosstalk Noise Voltage Estimation in the Victim Lines of Five-Coupled Interconnects

Since the state space matrices (E, A, B and C) derived in Chapter 2 for the two-coupled interconnects are in modular form, crosstalk estimation model can easily be extended to multi-coupled interconnect lines. This is illustrated by considering a set of five coupled interconnect lines each line with 5 RLGC sections as shown in figure 3.3.

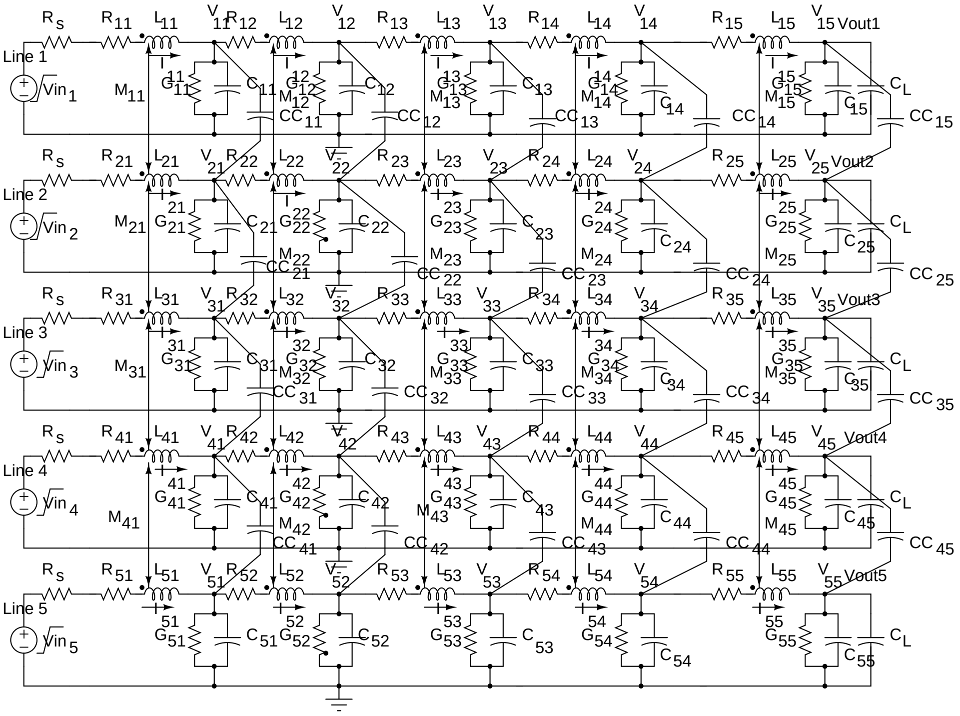


Figure 3.3: Five-coupled interconnects with 5 RLGC segments each

For this structure, the state space matrices are given by

$$\mathbf{E_{5coup}} = \begin{bmatrix} \mathbf{E_{c11}} & \mathbf{E_{c12}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{E_{21}} & \mathbf{E_{c22}} & \mathbf{E_{c23}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{E_{c32}} & \mathbf{E_{c33}} & \mathbf{E_{c34}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{E_{c43}} & \mathbf{E_{c44}} & \mathbf{E_{c45}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{E_{c54}} & \mathbf{E_{c55}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{E_{c66}} & \mathbf{E_{c67}} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{E_{c76}} & \mathbf{E_{c77}} & \mathbf{E_{c78}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{E_{c87}} & \mathbf{E_{c88}} & \mathbf{E_{c89}} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{E_{c98}} & \mathbf{E_{c99}} & \mathbf{E_{c910}} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{E_{c109}} & \mathbf{E_{c1010}} \end{bmatrix} \quad (3.3)$$

$$\mathbf{A_{5coup}} = \begin{bmatrix} \mathbf{A_{c11}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c16}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{A_{c22}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c27}} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{A_{c33}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c38}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c44}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c49}} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c55}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c510}} \\ \mathbf{A_{c61}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c66}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{A_{c72}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c77}} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{A_{c83}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c88}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c94}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c99}} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c105}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{A_{c1010}} \end{bmatrix} \tag{3.4}$$

$$\mathbf{B_{5coup}} = \begin{bmatrix} \mathbf{V_1} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \mathbf{V_2} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{V_3} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{V_4} & \mathbf{0} & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{V_5} & \mathbf{0} & \cdots & \mathbf{0} \end{bmatrix}^T \tag{3.5}$$

$$\mathbf{C_{5coup}} = \begin{bmatrix} \mathbf{0} & \cdots & \mathbf{0} & \mathbf{Vout1} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \cdots & \mathbf{0} & \mathbf{0} & \mathbf{Vout2} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \cdots & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{Vout3} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \cdots & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{Vout4} & \mathbf{0} \\ \mathbf{0} & \cdots & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{Vout5} \end{bmatrix} \tag{3.6}$$

State space matrices E and A for the structure shown in figure 3.3 are written from the generalized equations (2.26) and (2.27). Dimensions of E, A, B and C are 50×50, 50×50, 50×5 and 5×50 respectively. Each element in equations (3.3) to (3.6) is a matrix with a dimension of 5×5.

Equation (3.5) corresponds to the input signals applied to lines 1 to 5 (V_{in1} to V_{in5}) and equation (3.6) corresponds to the output signals seen at the other end of the lines 1 to 5 (V_{out1} to V_{out5}). Table 3.1 shows different input signal combinations, computed and measured peak noise voltages in the victim lines of the five-coupled interconnect system.

Consider Case 1 in table 3.1. A step signal of 1.8V is applied as input signal to Line

Table 3.1: Coupled noise voltages in the victim lines for different input switching combinations in the five-coupled interconnects

Case	V_1 (V)	V_2 (V)	V_3 (V)	V_4 (V)	V_5 (V)	Computed coupled peak voltage (mV) (using our model)	Coupled peak voltage (mV) (using SPICE simulation)
1	↑[1]	*Gnd*[2]	↑	Gnd	↑	V_2=506.4, V_4=506.4	V_2=506.2, V_4=506.2
2	↑	Gnd	↓[3]	Gnd	↑	V_2=118, V_4=118	V_2=117.9, V_4=117.9
3	↑	Gnd	↓	Gnd	↓	V_2=62.95, V_4=-493.3	V_2=63.23, V_4=-492.9
4	↑	↑	Gnd	↑	↑	V_3=551.9	V_3=553.4
5	↑	↑	Gnd	↓	↑	V_3=128.8	V_3=128.5
6	↑	↑	Gnd	↓	↓	V_3=0	V_3=0
7	↑	↓	Gnd	↓	↑	V_3=-398.1	V_3=-398.1
8	↑	↑	Gnd	Gnd	↑	V_3=327.8, V_4=320.3	V_3=327.8, V_4=319.9
9	↑	↓	Gnd	Gnd	↑	V_3=-182, V_4=234.9	V_3=-181.7, V_4=234.9
10	↑	↓	Gnd	Gnd	↓	V_3=-233.3, V_4=-304.9	V_3=-233.4, V_4=-305

↑[1] : Low (0V) to High (1.8V) transition
Gnd[2] : Input is connected to ground
↓[3] : High to Low transition

1, 3 and 5 (aggressor lines) and the coupled signal at nodes V_{out2} and V_{out4} of Line 2 and 4 (victim lines) is computed using the model. The model output is plotted along with the SPICE simulation in figure 3.4. Figure 3.5 shows the coupled noise voltages in the victim lines for Case 9 in table 3.1. From the plot shown in figures 3.4 and 3.5, it is found that model and SPICE responses are closely matching.

The state space matrices E, A, B and C for a general coupled network with k parallel interconnect lines and having m_i segments in i^{th} line ($m_i \geq k$) can easily be computed by simple programming technique. This approach is therefore modular in nature and hence can be extended to any general network. Further, in this type of crosstalk estimation, the model remains same for all input combinations unlike in other modeling approaches.

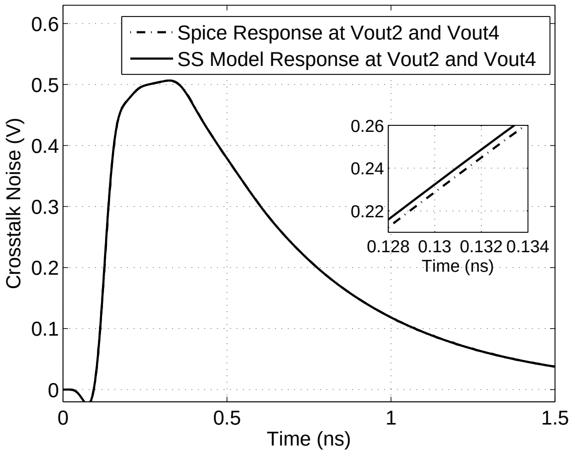


Figure 3.4: Comparison of state space model and SPICE responses of the coupled noise voltage in victim line 2 and 4 of the five-coupled interconnects (for case 1 in table 3.1)

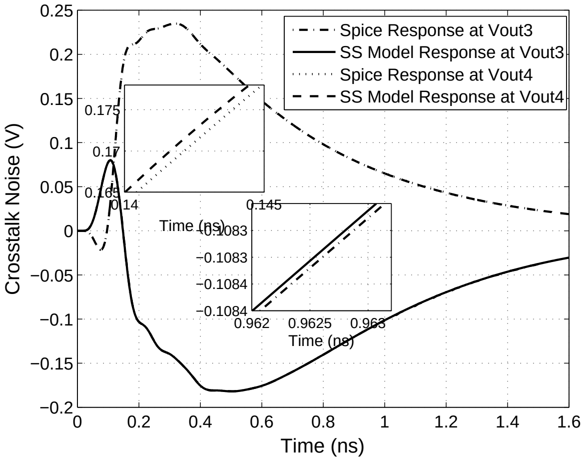


Figure 3.5: Comparison of state space model and SPICE responses of the coupled noise voltage in victim line 3 and 4 of the five-coupled interconnects (for case 9 in table 3.1)

3.1.4 Conclusions

Using state space matrices, coupled noise voltages in the victim line of the two-coupled interconnects is estimated. It is found that model response and SPICE response are closely matching. Since the elements of the derived state space matrices for the two-coupled interconnects are modular in nature, crosstalk estimation model can be easily extended to multi-coupled interconnect lines. This is illustrated by extending the model to five-coupled interconnect lines. Analysis on the crosstalk noise voltages in the victim lines of the five-coupled interconnects is carried out for different input switching combinations.

3.2 Model Order Reduction

3.2.1 Introduction

Ongoing drive in the VLSI industry for higher operating frequencies has made interconnects a dominant factor in the overall system performance. At high frequencies, interconnects behave as Multi-conductor Transmission Lines (MTLs). Mathematically, signal propagation behavior through the MTLs are described by partial differential equations. Usually, SPICE based circuit simulators are used to analyze the characteristics of the propagated signals through the interconnect lines.

To find the exact effects of interconnects on system performance, combination of extraction and analysis is used in todays IC chip design. Extraction of the interconnect lines determine the resistance (R), inductance (L), conductance (G) and capacitance (C), which can then be used to build a circuit model for the analysis of interconnect effects (Ratzlaff and Pillage, 1994). This often leads to a large equivalent circuit, whose simulation is computationally expensive and sometimes not feasible particularly in case of a large number of coupled lines. Model Order Reduction (MOR) has become a state of the art technique for fast simulation of the interconnect network parameters represented in the form of matrices with large dimensions reduced to smaller dimensions (Antoulas, 2005).

Distributed models of interconnect networks generally have large number of poles, spread over a wide-frequency range. Except for a few dominant poles, majority of the poles have very little effect on simulation results. In MOR technique, network containing large number of poles is reduced to smaller order which consists of only the dominant poles. One of the commonly used approaches to reduce the order of the model is the moment matching technique (Dumitriu and Iordache, 2007). In this work, moment matching method is used to reduce the order of the system using Pade approximation.

3.2.2 Order Reduction of the Distributed RLGC Network

3.2.2.1 Computation of Moments

Moment computation is defined as the recursive solving of an equivalent circuit in order to find the transfer function moments (coefficients of MacLaurin series of the transfer function) (Tan and He, 2007). In this work, interconnects are represented by distributed RLGC network and modeled using state space approach (Chapter 2). State space representation for the RLGC network is given in equation (2.22) and the generalized state space matrices for the single interconnect line having *n* RLGC sections is given in section 2.4.1. If the network has *n* RLGC sections, order of the network is *2n* and using MOR technique, this order can be reduced to q where $q << n$. The reduced system is represented as

$$\begin{aligned}\mathbf{E_r}\dot{\mathbf{x}}(t) &= \mathbf{A_r}\mathbf{x_r}(t)+\mathbf{B_r}\mathbf{u}(t)\\ \mathbf{y_r}(t) &= \mathbf{C_r}\mathbf{x_r}(t)\end{aligned} \tag{3.7}$$

The dimensions of the reduced state space matrices are $\mathbf{E_r} = q\times q$, $\mathbf{A_r} = q\times q$, $\mathbf{B_r} = q\times 1$ and $\mathbf{C_r} = q\times 1$.

Applying Laplace transformation to the equation (2.22) with null initial conditions, expression for the transfer function (H(s)) is given by,

$$H(s) = \mathbf{C}\left[\mathbf{E}s-\mathbf{A}\right]^{-1}\mathbf{B} = -\mathbf{C}\left[\mathbf{I}-s\mathbf{E}\mathbf{A}^{-1}\right]^{-1}\mathbf{B}\mathbf{A}^{-1} \tag{3.8}$$

Applying Taylors expansion for the term $[I - s\mathbf{E}\mathbf{A}^{-1}]^{-1}$ in equation (3.8), expression for H(s) becomes

$$H(s) = -\sum_{k=0}^{\infty} \mathbf{C}\mathbf{A}^{-(k+1)}\mathbf{B}\mathbf{E}^k s^k \tag{3.9}$$

Expanding the above equation,

$$H(s) = -\left[\mathbf{C}\mathbf{A}^{-1}\mathbf{B} + \mathbf{C}\mathbf{A}^{-2}\mathbf{B}\mathbf{E}s + \mathbf{C}\mathbf{A}^{-3}\mathbf{B}\mathbf{E}^2 s^2 + \cdots\cdots\right] \tag{3.10}$$

Equation (3.10) is expressed in terms of moments (m_k) as

$$H(s) = \sum_{k=0}^{\infty} m_k s^k \tag{3.11}$$

where m_k represents the moment vector and contains the moments of H(s) and defined as

$$m_k = -\mathbf{C}\mathbf{A}^{-(k+1)}\mathbf{B}\mathbf{E}^k s^k, k > 0 \tag{3.12}$$

3.2.2.2 Moment Matching Technique

Considering H(s) as the ratio of two polynomials, then

$$H(s) = \frac{a_0 + a_1 s + \cdots\cdots + a_{n-1}s^{n-1}}{1 + b_1 s + \cdots\cdots + b_n s^n} \tag{3.13}$$

It can be expressed in pole-residue form as

$$H(s) = c + \sum_{i=1}^{n_p} \frac{k_i}{s - p_i} \tag{3.14}$$

where n_p indicates the total number of circuit poles and c is the direct input-output coupling constant.

Number of poles in the transfer function of the interconnect increases with the number of RLGC sections and they in turn depend on the length of the interconnect. Thus obtaining a transfer function in the form of equation (3.14) becomes computationally expensive. MOR technique avoids this large computation by finding an approximate transfer function having a reduced order q which consists of only the dominant poles.

Moment Matching technique is used to obtain reduced model order with high accuracy (Celik *et al.*, 2002). The idea of Pade approximation is used to approximate the H(s) to an order limited rational function ($H_q(s)$) as

$$H_q(s) = \frac{a_0 + a_1 s + \cdots\cdots + a_{q-1} s^{q-1}}{1 + b_1 s + \cdots\cdots + b_q s^q} \tag{3.15}$$

where q is the order of the reduced system and $q << n$. Transfer function H(s) is represented as a Taylor series expansion as shown in equation (3.11). Once the moments are available, coefficients of the q^{th} reduced order model is obtained by matching its first $2q$ moments to the first $2q$ moments of the original circuit function (Tan and He, 2007) i.e.

$$H(s) = \frac{P(s)}{Q(s)} = \frac{a_0 + a_1 s + \cdots\cdots + a_{q-1} s^{q-1}}{1 + b_1 s + \cdots\cdots + b_q s^q} \tag{3.16}$$

Coefficients a_i and b_i are computed from equation (3.16) i.e.

$$\sum_{k=0}^{q-1} a_k s^k = \left(\sum_{k=0}^{2q-1} m_k s^k \right) \left(\sum_{k=0}^{q} b_k s^k \right) \tag{3.17}$$

Comparing the coefficients of s^q on both sides of equation (3.17), we have

$$m_0 b_q + m_1 b_{q-1} + \cdots\cdots + m_{q-1} b_1 + m_q = 0 \tag{3.18}$$

Applying this to the coefficients of s^q to s^{2q-1} yield a set of linear equations as

$$\begin{bmatrix} m_0 & m_1 & \cdots & m_{q-1} \\ m_1 & m_2 & \cdots & m_q \\ \vdots & \vdots & \vdots & \vdots \\ m_{q-1} & m_q & \cdots & m2q-2 \end{bmatrix} \begin{bmatrix} b_q \\ b_{q-1} \\ \vdots \\ b_1 \end{bmatrix} = - \begin{bmatrix} m_q \\ m_{q+1} \\ \vdots \\ m_{2q-1} \end{bmatrix} \tag{3.19}$$

Coefficients b_i of Q(s) in (3.16) are obtained by solving equation 3.19. Coefficients a_k are obtained by comparing the coefficients of s^q on the left and right hand side of equation (3.17) from s^0 to $s^{(q-1)}$ yields

$$\begin{bmatrix} a_0 \\ a_1 \\ \vdots \\ a_{q-1} \end{bmatrix} = \begin{bmatrix} m_0 & 0 & 0 & \cdots & 0 \\ m_1 & m_2 & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ m_{q-1} & m_{q-2} & m_{q-3} & \cdots & m0 \end{bmatrix} \begin{bmatrix} 1 \\ b_1 \\ \vdots \\ b_{q-1} \end{bmatrix} \tag{3.20}$$

Reduced transfer function $H_q(s)$ is formulated from the above coefficients a_i and b_i.

3.2.3 Simulation Results

In this work, interconnects are represented by distributed RLGC network as shown in figure 2.13. Simulations are performed for an RLGC network of size 100×100 and moment matching technique is applied to reduce the system to a size n×n with n=2, 3, 4, 5 etc. and the respective responses are plotted. In general, a system matrix of fairly large dimensions can be quickly reduced to a smaller dimension without compromising the accuracy of the results.

Using moment matching technique, RLGC network of size 100×100 is reduced to 7×7, 6×6, 5×5, 4×4 size. Transfer function of the reduced models is obtained using Matlab functions. With step signal as input, transient response for the reduced models is obtained. Above results are compared with actual SPICE simulation results. It is observed from figure 3.6 that the order 7 response closely resembles with the response of the original model of order 100.

3.2.4 Conclusions

In this work, model order reduction technique is applied to reduce the interconnect of large order RLGC network in DSM technologies. Moment matching method is used to get a close approximation of the original transfer function. Time domain responses of the reduced models of different orders are obtained and are compared. In the example presented above, it is shown that the order 7 response closely resembles with the

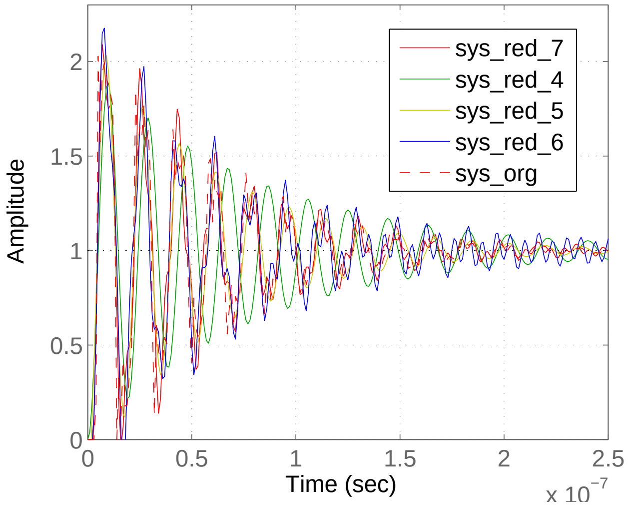


Figure 3.6: Response of the original and reduced models

response of the original model of order 100.

CHAPTER 4

Delay and Crosstalk Reduction in Resonant High Speed On-Chip Interconnect Lines

4.1 Introduction

As stated before, advances in VLSI technology and aggressive scaling redefines in many ways, the role of interconnects vis-á-vis logic in determining the overall performance of integrated circuits. Long interconnects play a vital role in DSM regime ICs and introduce signal integrity issues such as delay, crosstalk, power dissipation etc. Because of these reasons, long interconnects have become the performance bottlenecks and require a relook at mitigating these effects at different levels of circuit design.

Several circuit oriented techniques have been developed to reduce the delay in long on-chip interconnects. Some of the previously used most popular techniques are repeater insertion, differential signaling, current mode signaling etc. Repeater insertion reduces the propagation delay dependency from quadratic to linearity with the interconnect length (Bakoglu and Meindl, 1985). Expression to find the optimum number of repeaters for an interconnect represented using an RLC model is derived in (Ismail and Friedman, 1998). Optimizing the interconnect geometries for minimum delay, taking inductive effects into consideration, are discussed in (El-Moursy and Friedman, 2004). In (El-Moursy and Friedman, 2007), it is shown that tapering of the interconnects reduces the propagation delay by 15% and power dissipation by 16%. In addition to these, several circuit techniques with the optimum device dimension approaches to reduce interconnect delay have been published. But, in all these techniques, as the length of the interconnects increases, more and more number of repeaters have to be inserted to reduce the overall delay and this results in significant increase in power dissipation and area overhead.

To reduce power dissipation, low voltage signaling schemes are suggested (Dhaou *et al.*, 2001). With the increase in frequency of operation, several signal integrity problems coupled with the need for high bandwidth interconnects is increased. As the voltage signaling is not able to produce the required bandwidth, current mode signaling was proposed (Maheshwari and Burleson, 2001). In (Valentian and Amara, 2004), current mode signaling technique is used to transmit high data rate signals. To improve the delay and power dissipation, current mode sense amplifier is proposed at the receiving end (Tzartzanis and Walker, 2005). But current mode circuits suffer from static power dissipation. Despite their stated advantages, all these techniques suffer from the limited bandwidth capability, resulting in speed bottlenecks for high speed operation.

The concept of exploiting standing waves in a transmission line is first proposed in (Chi, 1994). Global resonant clock distribution network is developed by using this concept with a set of external spiral inductors and capacitors attached to the H-tree structure (Chang *et al.*, 2003). The capacitance of the clock distribution network resonates with the inductance and on-chip capacitors establish a mid-rail DC voltage around which the grid oscillates. This approach lowers the power consumption, skew, and jitter. In this paper, the authors claim that at lower frequencies of operation, resistive part of the interconnect is dominant and behaves as distributed RC network. At higher frequencies of operation, interconnect behaves as distributed LC network due to the dominating inductive component of the line. Phase Shift Keying (PSK) modulation is used to illustrate this concept by transmitting a 1 GHz data over a 7.5 GHz carrier. However, this type of modulation resulted in large power dissipation and poor spectral efficiency.

To mitigate the dispersion loss at high frequencies, Return to Zero (RZ) modulation scheme is used in which sharp current pulses are used to transmit the data in (Jose *et al.*, 2005). The transmitted data is modulated to higher frequencies by maximizing the effect of wire inductance and this approach reduces the dispersion loss to a certain extent.

As an alternative to electrical interconnects and to overcome from electrical related limitations, optoelectronic links are used as the media for communication for on-chip signals (Kyriakis Bitzaros *et al.*, 2001). Optical interconnections promise to achieve high bandwidth and provide high density parallel communication channels. However, interface between the electrical and optical signals is a major issue in optoelectronic applications.

Demand for low power techniques brought the concept of quasi-resonant interconnects (Rosenfeld and Friedman, 2009). The idea is to make a resonating interconnect by inserting an inductor of appropriate value along the interconnect so as to make the interconnect capacitance to resonate around the fundamental frequency of the signal. As the circuit ("interconnect") is under resonance, energy resonates between electric and magnetic fields rather than dissipating as heat. This reduces the power dissipation as well as the delay introduced by the interconnect to a minimum. This eliminates the need for inserting buffers along the interconnects to reduce the delay.

In (Rosenfeld and Friedman, 2009), quasi resonant interconnect network is developed by inserting a passive inductor at a specific point in the interconnect line so as the network resonates at a desired frequency for minimum delay and power dissipation. In this paper, on-chip passive inductor is implemented in planar spiral octagonal shape. Main drawbacks of using passive inductors include large area overhead and large parasitics associated with the structure. Also, quality factor of the passive inductors is small and is not tunable for different data rates. In addition to this, physical dimensions of the spiral inductors are directly related to the inductance values. As the passive inductance value increases, the area required to fabricate also increases proportionally.

Further, in GHz frequency regime, on-chip intermediate/global interconnects behave as transmission lines. Interconnects in an IC run parallel to each other and exhibit inductive and capacitive coupling between closely placed lines. This results in the performance degradation due to the induced crosstalk noise voltage in the neighboring lines((Eo and Eisenstadt, 1993), (Ismail *et al.*, 1999), (Davis and Meindl, 2000)).

Active inductors provide an attractive alternative in terms of less area, less number of stray components, tunability, high quality factor and easier floor planning in comparison to the spiral inductors. This work presents the use of an active inductor configuration with resistance in the feed-forward path in place of an on-chip passive inductor. This arrangement can be referred to as Resonant Interconnect Network (RIN). A small resistance in the feedforward path of the active inductor is used to increase the output voltage swing. Gyrator-C configuration is used to design the floating active inductor. The performance comparison and improvements as far as power dissipation, delay and area are concerned by using an active inductor in place of a passive inductor are presented. Further, analysis and comparison of the coupled crosstalk noise voltage on the victim line of the coupled resonant interconnect sections is also presented.

4.2 Principle of Resonant Interconnect Network (RIN)

RIN system with active inductor as the resonating element is shown in figure 4.1. Transmitter at the near end of the interconnect modulates the input data signal and modulation supports periodic signal with a single resonant frequency. Transmitter is followed by an inverter driving the interconnect. The RLGC distributed transmission line is separated by an on-chip active inductor (L_s) inserted at a specific point to resonate at a desired frequency for minimum power consumption and interconnect delay. Resistance in the feed-forward path of the active inductor helps to obtain full rail-to- rail output voltage swing. The receiver at the far end of the interconnect demodulates the transmitted signal back to the original input bit stream.

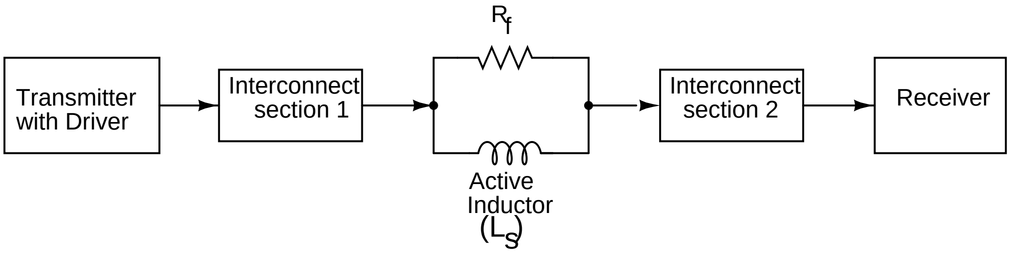


Figure 4.1: RIN system

Since the fundamental harmonic component of the input signal is amplified by the magnitude of the transfer function, the network resonates at a specific target frequency and magnitude. This behavior is required to transfer a full swing sinusoidal signal at the resonant frequency to the far end of the interconnect. To illustrate this, consider the output signal in the frequency domain, (Rosenfeld, 2009)

$$V_{out}(s) = H_1(s)V_{in}(s) \tag{4.1}$$

where $H_1(s)$ is the transfer function of the network between the transmitter and the receiver including the driver and $V_{in}(s)$ is the input data. Assuming the input data signal as periodic, its Fourier series representation is given by

$$V_{in}(t) = \sum_{k=-\infty}^{\infty} a_k e^{jk\omega_p t} \tag{4.2}$$

where a_k is the k^{th} harmonic of the signal and ω_p is the resonant frequency. The fundamental harmonic component of a periodic square wave signal is given by

$$a_1 = \pm \frac{V_a t_p}{2t_r\pi^2}(e^{-j\omega_p t_p} - 1) \tag{4.3}$$

where V_a, a_1, t_p and t_r denote amplitude, first fundamental harmonic component, period and rise time of the pulse signal respectively. The magnitude of the transfer function can be obtained using equation (4.1) as,

$$|H_1(j\omega_p)| = \frac{V_a/2}{2|a_1|} = \frac{V_a}{4a_1} \tag{4.4}$$

Substituting equation (4.3) into (4.4), we get

$$|H(j\omega_p)| = \frac{t_r\pi^2}{t_p\sqrt{8(1-cos(\omega_p t_r))}} \tag{4.5}$$

Equation (4.5) describes the magnitude of the transfer function at the resonant frequency ω_p. For example, at ω_p=2 GHz and t_r=10 *ps*, the magnitude of the transfer function is computed as 0.8.

4.3 Modeling the RIN Section

Resonant frequency of the system in figure 4.1 is found by replacing the transmitter by a voltage source (V_{in}) in series with a resistance (R_d) and the receiver section by a capacitive load (C_L) as shown in figure 4.2. Analysis of the RIN network is carried out by replacing the interconnects with distributed RLGC network along with the active inductor in series as shown in figure 4.2. Floating active inductor design and its equivalent model is given in the next section.

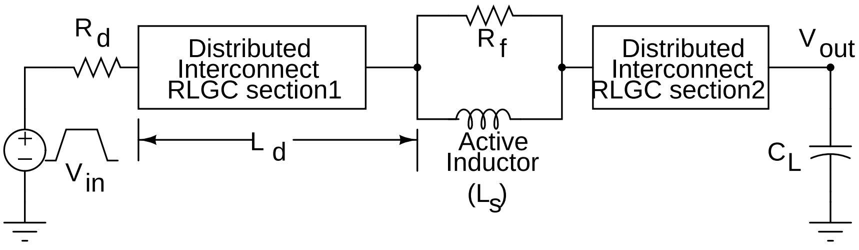


Figure 4.2: RIN section modeling

4.3.1 Introduction to Active Inductors

CMOS inductor circuits are the active networks built using MOS transistors. Under certain DC biasing conditions and signal-swing constraints, these circuits exhibit inductive characteristic for a range of frequencies. Gyrator network with capacitors is one of the widely used configurations of an active inductor.

4.3.1.1 Principle of Single-Ended and Floating type Active Inductors

Gyrator-C is a well known circuit topology used to synthesize an active inductor. This configuration consists of two back-to-back connected transconductors and a capacitor connected to one of the ports as shown in figure 4.3 (Yuan, 2008). This topology is said to be lossless when both the input and output impedances of the transconductors of the network are infinite and the transconductance values are constant. The admittance

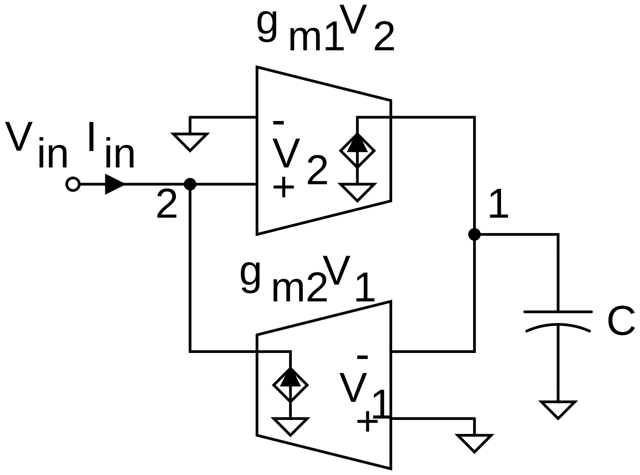


Figure 4.3: Singe-ended gyrator-C active inductor configuration

looking from port 2 in figure 4.3 is given by

$$Y = \frac{I_{in}}{V_2} = \frac{1}{(\frac{C}{g_{m1}g_{m2}})} \tag{4.6}$$

where g_{m1} and g_{m2} indicate the transconductance of transconductors 1 and 2 respectively. Equation (4.6) indicates that port 2 of the gyrator-C network behaves as a single-ended lossless inductor with an inductance of,

$$L = \frac{C}{g_{m1}g_{m2}} \tag{4.7}$$

Floating type active inductor is designed by replacing single ended transconductors in figure 4.3 with differentially configured transconductors. A lossy floating active inductor (input and output impedances of the transconductors are finite) is shown in figure 4.4. In a floating inductor, terminals of the inductor are not connected either to the ground or to the power supply of the circuit. Applying KCL at nodes 1+, 1-, 2+ and 2- in figure 4.4 gives,

$$-g_{m1}\left(V_2^+ - V_2^-\right) + \left(\frac{sC_1 + G_{01}}{2}\right)\left(V_1^- - V_1^+\right) = 0 \tag{4.8}$$

$$I_{in} + \left(\frac{sC_1 + G_{02}}{2}\right)\left(V_2^- - V_2^+\right) + g_{m2}\left(V_1^+ - V_1^-\right) = 0 \tag{4.9}$$

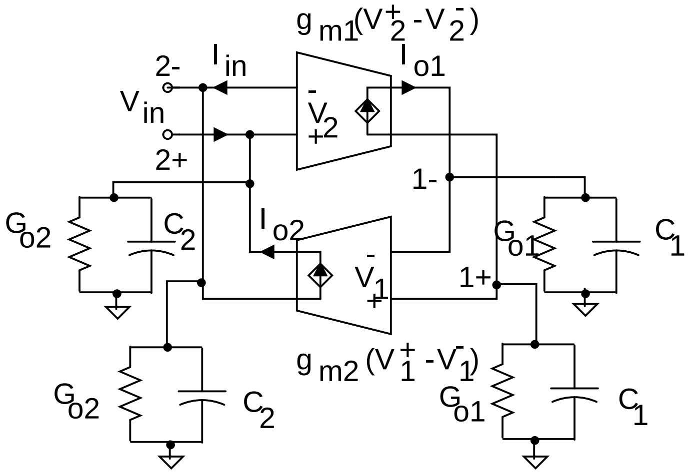


Figure 4.4: Floating gyrator-C active inductor configuration

where G_{01}, C_1, G_{02} and C_2 denote the conductances and the capacitances at nodes 1 and 2 respectively. V_1^+, V_1^-, V_2^+ and V_2^- indicate the voltages associated with the nodes 1^+, 1^-, 2^+ and 2^- respectively. The admittance looking from port 2 in figure 4.4 is given by,

$$Y = \frac{I_{in}}{V_2^+ - V_2^-} \tag{4.10}$$

Substituting for (V_2^+-V_2^-) in equation (4.10) from equations (4.8) and (4.9), we get

$$Y = s\frac{C_2}{2} + \frac{G_{02}}{2} + \frac{1}{s\left(\frac{C_1}{2g_{m1}g_{m2}}\right) + \frac{G_{01}}{2g_{m1}g_{m2}}} \tag{4.11}$$

Equation (4.11) can be represented by an RLC network as shown in figure 4.5 with its parameters given as,

$$R_p = \frac{2}{G_{o2}} \tag{4.12}$$

$$C_p = \frac{C_2}{2} \tag{4.13}$$

$$R_s = \frac{G_{01}/2}{g_{m1}g_{m2}} \tag{4.14}$$

$$L_s = \frac{C_1/2}{g_{m1}g_{m2}} \tag{4.15}$$

Floating active inductor equivalent circuit shown in figure 4.5 behaves as a lossy

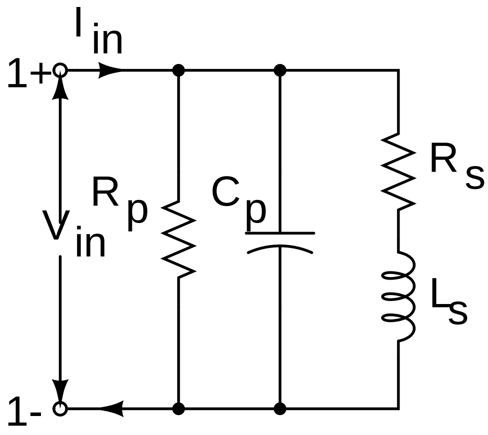


Figure 4.5: RLC equivalent circuit of the floating active inductor

inductor with its parallel parasitic resistance (R_p), parallel capacitance (C_p) and series resistance (R_s). To reduce the ohmic losses of the active inductor, R_p should be maximized while R_s should be minimized. From equations (4.12) to (4.15), we observe that R_p and C_p depends only on G_{o2} and C_2 while G_{01} and C_1 affects R_s and L_s.

4.3.1.2 Operating Frequency Range of Active Inductors

The active inductor circuit exhibits an inductive characteristic only over a specific frequency range. Input impedance analysis of the circuit gives the inductive frequency range of operation. Figure 4.6 shows a general impedance response plot of a floating active inductor circuit (Yuan, 2008). From the plot, it is observed that the circuit is resistive when $\omega < \omega_z$, inductive when $\omega_z < \omega < \omega_0$ and capacitive when $\omega > \omega_0$, where ω indicates the frequency in radians. Equations (4.12) and (4.14) show that R_p has no effect on the frequency range while R_s affect the lower bound of the frequency range over which the gyrator-C network is inductive. The upper bound of the frequency range is set by the self resonant frequency of the active inductor which is set by the cut-off frequency of the transconductors constituting the active inductor. For a maximum active inductance (L_s), both R_s and C_p should be minimized.

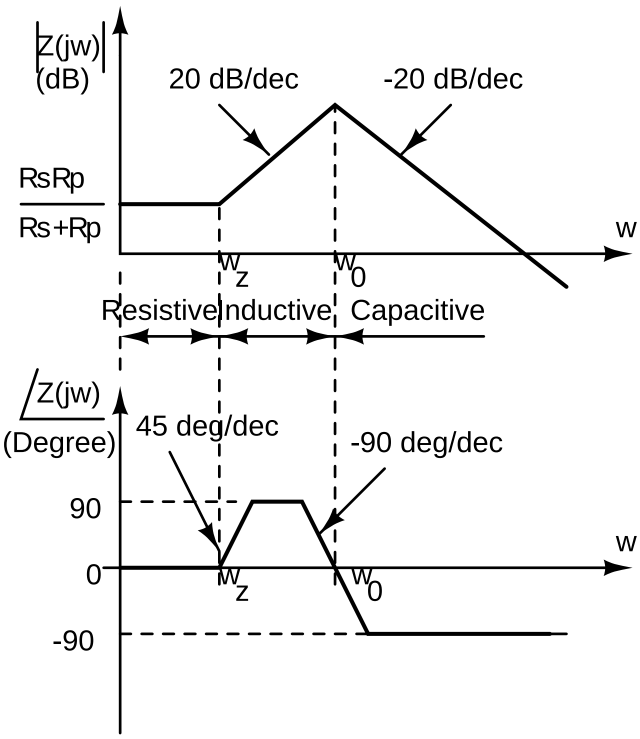


Figure 4.6: General impedance response of a floating active inductor circuit (Yuan, 2008)

4.3.1.3 Quality Factor (Q)

Q of an inductor is defined as the ratio of the net magnetic energy stored to its ohmic loss in one oscillation cycle. For spiral inductors, Q is independent of the voltage or current of the inductors. This property, however, does not hold for active circuits as the inductance depends upon the transconductances of the transconductors and the load capacitances. The power dissipated by the active inductor circuit is given by

$$P(j\omega) = I(j\omega)V^*(j\omega) = Re[Z]\,|I(j\omega)|^2 + jIm[Z]\,|(j\omega)|^2 \tag{4.16}$$

where $Re[Z]$ and $Im[Z]$ indicate the resistive and inductive reactances of the inductor respectively. $V(j\omega)$ and $I(j\omega)$ denote the voltage across and the current through the inductor respectively. The superscript $*$ denotes the complex conjugation and $|\cdot|$ indicates the absolute value operator. The first term in equation (4.16) quantifies the net energy loss arising from the parasitic resistances of the active inductor circuit whereas the second term measures the magnetic energy stored in the inductor. Hence the quality factor of the circuit is given by

$$Q = \frac{Im\left[Z\right]}{Re\left[Z\right]} \tag{4.17}$$

4.3.2 Implementation of Active Inductor Circuits

In RIN section, active inductor is inserted at a specific point in the interconnect line as shown in figure 4.2. Henceforth, active inductor is to be of floating type and constructed using differential transconductor configuration. Active inductor topology of good quality factor and operating in GHz regime is the need of the design. Different active inductor circuits are analyzed and the details are given below.

4.3.2.1 Mahmoudi-Salama Floating Active Inductor

The schematic of Mahmoudi-Salama floating active inductor is shown in figure 4.7 (Mahmoudi and Salama, 2005). The circuit consists of a pair of differential transconductors and a pair of negative resistors. Transistors M_8 and M_{16} biased in the triode region and connected across the outputs of the transconductors provides the tunability of the negative resistance values without using a tail current source.

Input impedance magnitude, phase and Q plots of the Mahmoudi-Salama floating active inductor are shown in figures 4.8, 4.9 and 4.10 respectively. For clarity, the frequency sweep in different plots is represented either in log scale or in linear scale depending upon the parameter of interest. In this active inductor configuration, the maximum Q is very low and hence this configuration is not suitable for the intended use.

4.3.2.2 Grozing Floating Active Inductor

The schematic of Grozing floating active inductor is shown in figure 4.11 (Grozing *et al.*, 2001). The circuit employs two basic differential-pair transconductors. Two

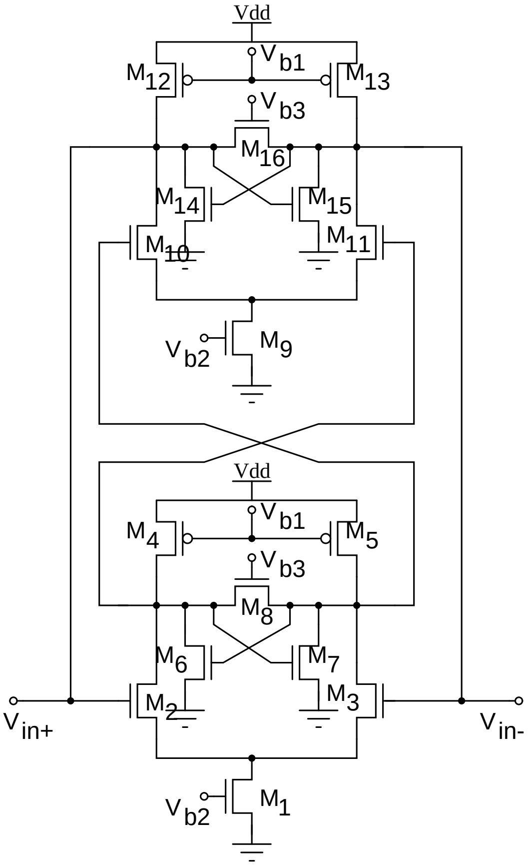


Figure 4.7: Schematic of Mahmoudi-Salama floating active inductor

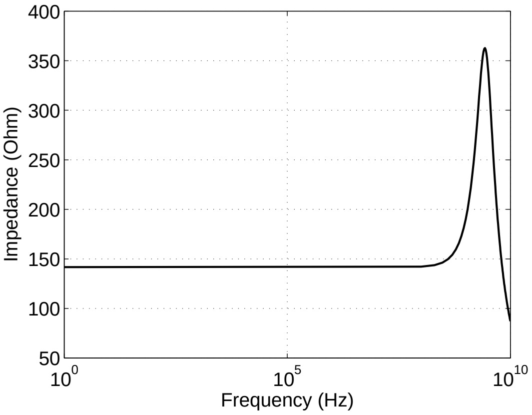


Figure 4.8: Input impedance of Mahmoudi-Salama floating active inductor

negative resistors are connected across the output nodes of the transconductors to cancel out the parasitic resistances of the active inductor. The inductance of the active inductor is tuned by varying the transconductances of the transconductors. Transconductances are changed by adjusting the tail currents of the differential pairs J_1 and J_2. The current

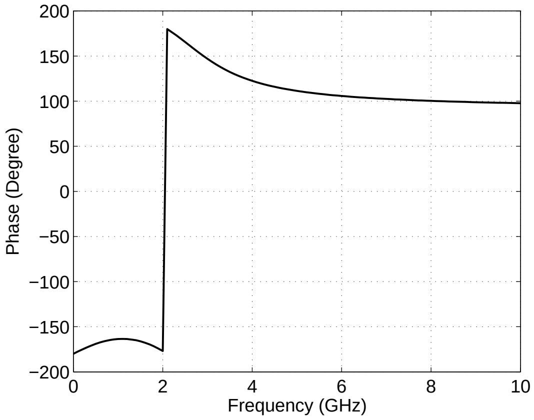


Figure 4.9: Phase response of Mahmoudi-Salama floating active inductor

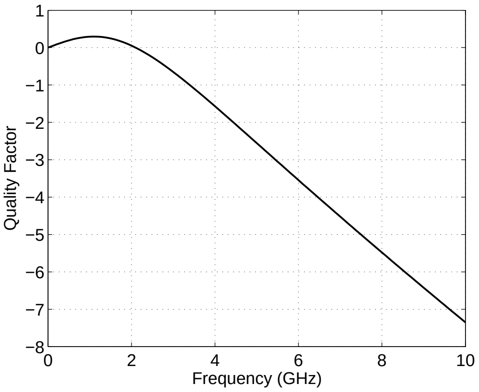


Figure 4.10: Quality factor of Mahmoudi-Salama floating active inductor

sources J_1, J_2, J_3 and J_4 are implemented using current mirror circuits. The quality factor of the active inductor is tuned by varying the resistances of the negative resistors.

Input impedance magnitude and phase plots of the Grozing floating active inductor are shown in figures 4.12 and 4.13. Quality factor versus frequency plot of the Grozing inductor is shown in figure 4.14. Even though the Q of this active inductor is good (around 250 at 1.6 GHz), input impedance of the circuit is quite large at this frequency (approximately 1800 Ω). In addition to this, circuit has a large size and maintaining four constant current sources is very difficult from the design and power dissipation perspective. Hence, this circuit does not suit well for the present application.

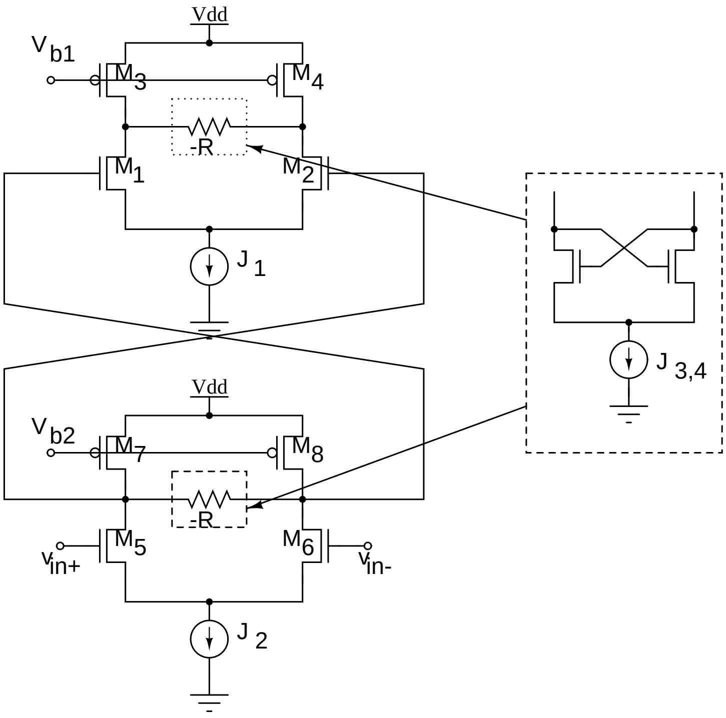


Figure 4.11: Schematic of Grozing floating active inductor

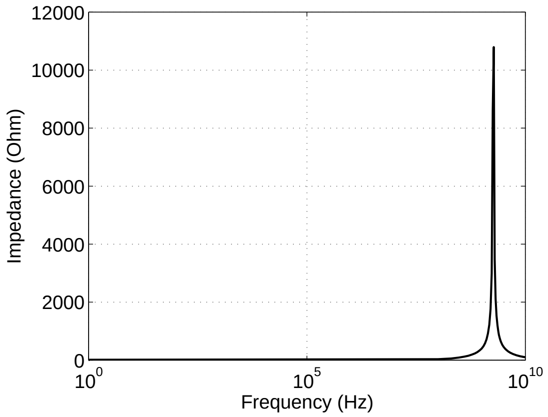


Figure 4.12: Input impedance of Grozing floating active inductor

4.3.2.3 Lu Floating Active Inductors

Lu floating active inductor is implemented as shown in figure 4.15 (Lu *et al.*, 2006). In this circuit, transistors M_1 and M_2 form a cross coupled pair while M_3 and M_4 are in the common drain configuration. Current sources J_1 and J_2 will help to maintain a constant drain current in the transistors M_3 and M_4 and are implemented using current mirror circuits. At the quiescent bias point, transistors M_1 to M_4 operate in the saturation

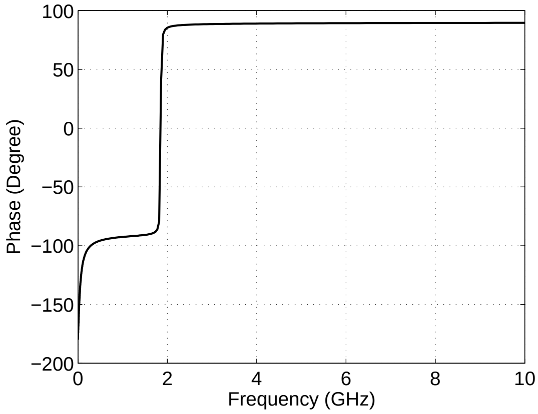


Figure 4.13: Phase response of Grozing floating active inductor

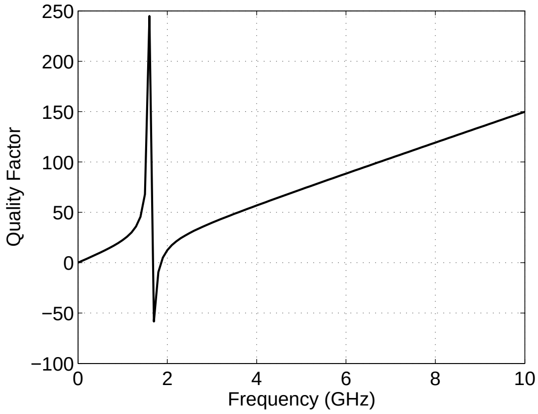


Figure 4.14: Quality factor of Grozing floating active inductor

region. Transistors M_5 and M_6 operate either in the saturation or in the linear region depending on the control voltage (V_b) applied to the gate terminal of these transistors.

Input impedance magnitude, phase and Q plots of the Lu floating active inductor are shown in figures 4.16, 4.17 and 4.18 respectively. Quality factor of the circuit is around 50 at 2 GHz with the input impedance of 75 Ω at this frequency. The circuit is inductive for reasonably good frequency range (500 MHz to 8 GHz). These characteristics are good-enough for the present application and can be used as an active inductor in high speed transmission lines. Hence, this topology is further analyzed for the tunability aspect and the robustness of the inductance values.

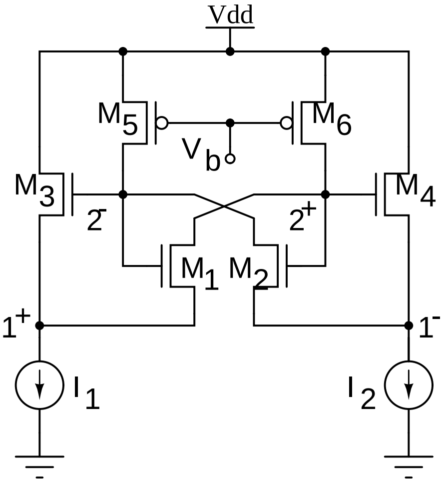


Figure 4.15: Schematic of Lu floating active inductor configuration

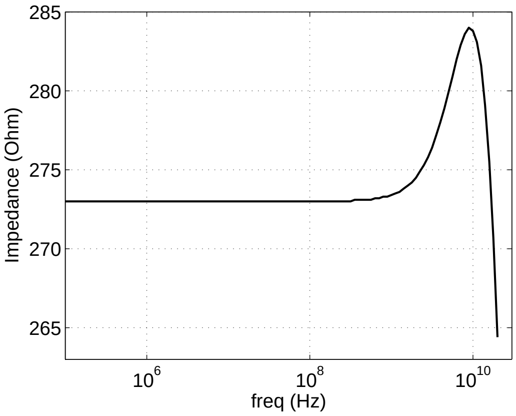


Figure 4.16: Input impedance of Lu floating active inductor

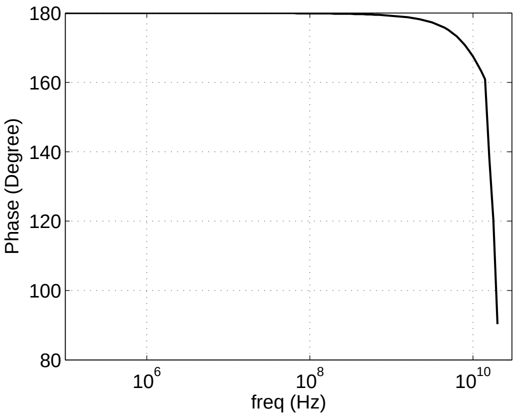


Figure 4.17: Phase response of Lu floating active inductor

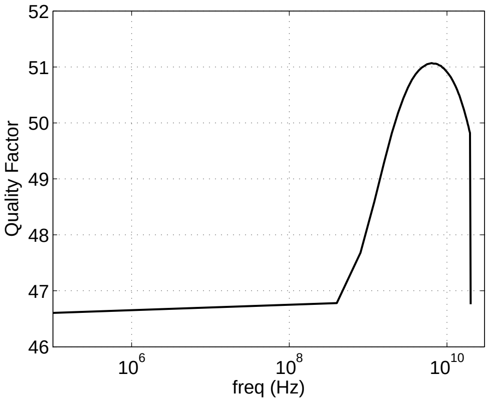


Figure 4.18: Quality factor of Lu floating active inductor

4.3.2.4 Analysis of Lu Floating Active Inductor Characteristics

Small signal analysis of the circuit in figure 4.15 gives the expression for the impedance at the differential input port (at nodes 1^+ and 1^-) as

$$Z_{in} = \frac{2[s(C_{gs1}+C_{gs3})-g_{m1}+g_{ds5}]}{g_{ds5}(g_{m1}+g_{m3}+s(C_{gs1}+C_{gs3}))} \tag{4.18}$$

where g_{m1}, C_{gs1}, g_{m3} and C_{gs3} indicate the transconductance and gate capacitances of the transistors M_1 and M_3 respectively The drain conductance of transistor M_5 is denoted by g_{ds5}. If $(2g_{m1}+g_{m3}) > g_{ds5}$, input impedance of the differential active inductor can be approximated to the model shown in figure 4.5 where

$$R_p = \frac{2}{g_{ds5}} \tag{4.19}$$

$$R_s = \frac{2(g_{ds5}-g_{m1})}{g_{ds5}(2g_{m1}+g_{m3}-g_{ds5})} \tag{4.20}$$

$$L_s = \frac{2(C_{gs1}+C_{gs3})}{g_{ds5}(2g_{m1}+g_{m3}-g_{ds5})} \tag{4.21}$$

$$C_p = \frac{C_{gs3}}{2} \tag{4.22}$$

Using equations (4.17) and (4.18), expression for Q of the active inductor circuit is computed as

$$Q = \frac{j\omega(C_{gs1}+C_{gs3})(2g_{m1}+g_{m3}-g_{ds5})}{(g_{m1}+g_{m3})(g_{ds5}-gm1)+\omega^2(C_{gs1}+C_{gs3})^2} \tag{4.23}$$

If the control voltage applied to the gate of the transistors M_5 and M_6 is varied, the reactance of the circuit changes. To know the range of variations in the reactance, V_b is varied in steps of 40 mV and is plotted as shown in 4.19. If the value of V_b is above some limit, the circuit will not have the inductive operating region. This can be observed in figure 4.20 when the applied V_b for the transistors M_5 and M_6 is 800 mV.

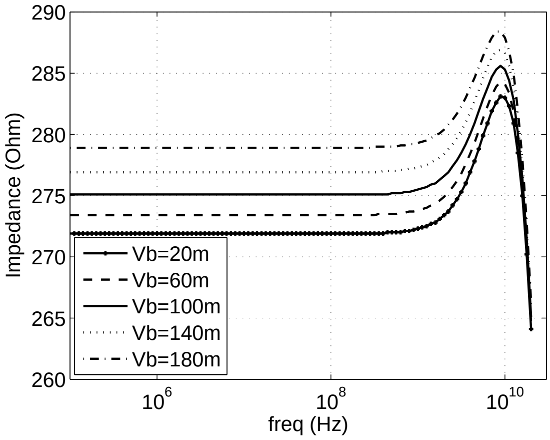


Figure 4.19: Variation in the reactance of the circuit for different control voltages

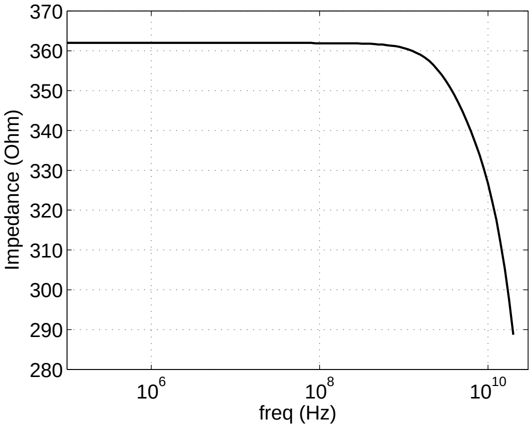


Figure 4.20: Active inductor impedance response when the applied control voltage is outside the acceptable range (V_b=800 mV)

The variation of active inductance values for different drain conductances of transistors M_5 and M_6 for a constant applied V_b is shown in figure 4.21. The inductance of the circuit varies from 9 nH to 1 nH when the width of the transistors M_5 and M_6 is changed from 0.5 μm to 1.3 μm. In figure 4.21, it can be seen that the inductance of the circuit is set to 7.5 nH at 2 GHz when the width of the transistors M_5 and M_6 is 0.7 μm.

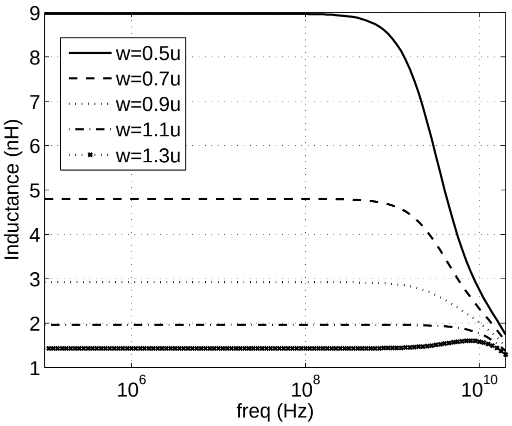


Figure 4.21: Variation of inductance for different widths of transistors M_5 and M_6

4.3.3 Mathematical Model of a RIN Section using State Space Approach

Mathematical equivalent model for each block of the RIN section in figure 4.2 is derived using state space approach. The equivalent circuit and corresponding state space matrices are given in the following sections.

4.3.3.1 Reduced Order State Space Matrices for the Interconnect Section

In Chapter 2, interconnects are represented by distributed RLGC network model and a method to compute the interconnect metrics using State Space approach is presented. Intermediate and global interconnects often have long lengths and their equivalent circuits consist of large RLGC sections. Simulation of these large equivalent circuits is computationally expensive and sometimes not feasible particularly in case of large number of coupled lines. Circuit containing large RLGC sections have large number of poles. Model order reduction technique restricts the poles only to dominant ones (section 3.2). In figure 4.2, each interconnect section is reduced to an equivalent second order network with corresponding state space matrices as,

$$E_{int} = \begin{bmatrix} L_{int} & 0 \\ 0 & C_{int} \end{bmatrix} \tag{4.24}$$

$$A_{int} = \begin{bmatrix} -R_{int} & -1 \\ 1 & 0 \end{bmatrix} \tag{4.25}$$

$$B_{int} = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \tag{4.26}$$

$$C_{int} = [0 \quad 1] \tag{4.27}$$

$$D_{int} = [0] \tag{4.28}$$

4.3.3.2 State Space Model for the Active Inductor

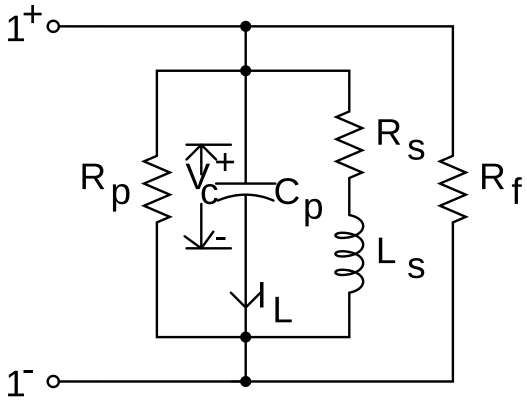


Figure 4.22: Active inductor equivalent circuit with resistance in feedforward path

Figures 4.2 shows the RIN section employing active inductor and figure 4.22 shows the equivalent circuit of the active inductor with a resistance in the feedforward path. Loop equations are applied to the circuit shown in figure 4.22 by considering a small load resistance R_L between node 1^- and ground. Corresponding state space equations are,

$$L_s \frac{dI_L(t)}{dt} = V_c - I_L(t) R_s \tag{4.29}$$

$$C_p \frac{\mathrm{d}V_c}{\mathrm{d}t} = \frac{V_1^+}{2R_L} - V_c \left[\frac{1}{2R_L} + \frac{R_f + R_p}{R_p R_f} \right] - I_L(t) \tag{4.30}$$

where V_1^+ and V_1^- are the voltages associated with the nodes 1^+ and 1^- respectively. Accordingly the state space matrices are given by,

$$E_{act\_ind} = \begin{bmatrix} L_s & 0 \\ 0 & C_p \end{bmatrix} \tag{4.31}$$

$$A_{act\_ind} = \begin{bmatrix} -R_s & 1 \\ -1 & -\left(\frac{1}{2R_L} + \frac{R_f + R_p}{R_f R_p} \right) \end{bmatrix} \tag{4.32}$$

$$B_{act\_ind} = \begin{bmatrix} 0 \\ \frac{1}{2R_L} \end{bmatrix} \tag{4.33}$$

$$C_{act\_ind} = \begin{bmatrix} 0 & -1 \end{bmatrix} \tag{4.34}$$

$$D_{act\_ind} = [1] \tag{4.35}$$

4.4 Characteristics of the RIN Section

To test the transient characteristics and delay in the RIN section employing active inductor configuration, simulations are carried out using *0.18* μm CMOS technology in Cadence Virtuoso. For the simulations, clock period (t_p), rise time (t_r), supply voltage (V_{DD}), load capacitance (C_L) and interconnect length (l) are chosen as 500 *ps*, 10 *ps*, 1.8 V, 100 fF and 10 *mm* respectively. Interconnect parasitics (per milli-meter) resistance (R), inductance (L), conductance (G), capacitance (C), coupling capacitance (CC) coefficient and mutual inductance (M) coefficient are chosen as 15.8 Ω/mm, 1.36 nH/mm, 9 $\mu\mho/mm$, 62 fF/mm, 0.6 and 0.5 respectively (NIMG, 2008).

4.4.1 Simulation of the RIN Section

The active inductor is inserted at a distance L_d (figure 4.2) from the transmitter , to resonate at the frequency of the data signal being transmitted in such a way that minimum power-delay product is achieved. Figure 4.23 shows that the power delay product is minimum for the inductance value of 7.5 *nH* when it is inserted at a distance of 8.5 *mm* from the starting point of the interconnect.

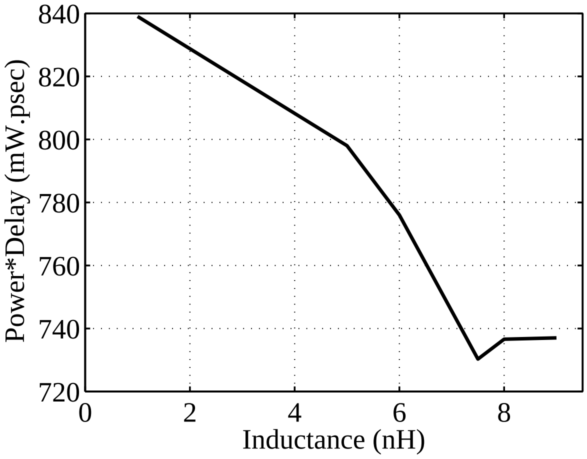


Figure 4.23: Minimum power delay product as a function of inductance

Magnitude response of the RIN section is shown in figure 4.24 and it is found that the resonance of the section occurs at 2.32 GHz (as seen from the maximum magnitude) while the theoretical resonant frequency is 2.0 GHz as determined from equation (4.5). This small shift in the resonant frequency can be attributed to the parasitic capacitance of the on-chip active inductor.

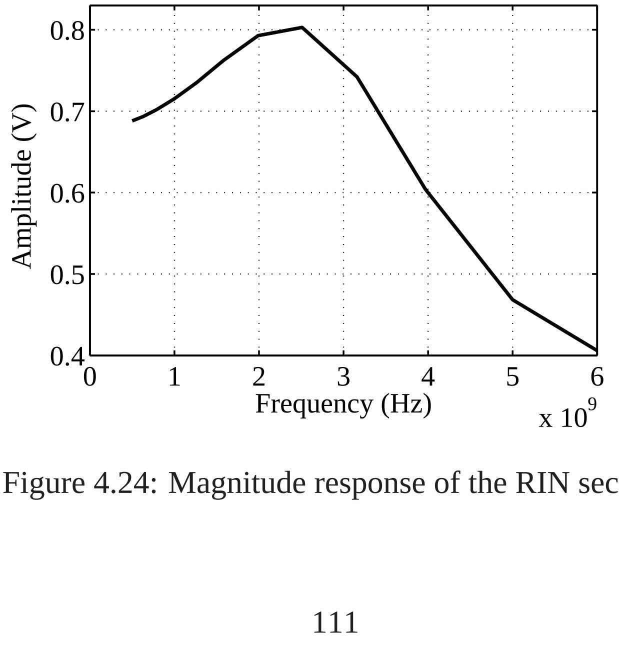


Figure 4.24: Magnitude response of the RIN section

4.4.2 Delay Estimation in RIN Section

Mathematical model for the interconnect section and active inductor is derived in section 4.3.3. Note that the RIN section consists of 3 blocks (an active inductor block in between two interconnect blocks as shown in figure 4.2) and the transfer function of each block can be represented as,

$$H_i(s) = C_i(sI - A_i)^{-1}B_i \tag{4.36}$$

where A_i, B_i and C_i denote the state space matrices of each block and I is the identity matrix. Overall transfer function of the RIN section ($H_T(s)$) is the product of individual transfer functions of each block. i.e.

$$H_T(s) = H_{int1}(s) \times H_{act\_ind}(s) \times H_{int2}(s) \tag{4.37}$$

where $H_{int1}(s)$, $H_{act\_ind}(s)$ and $H_{int2}(s)$ are the transfer functions of first interconnect section, active inductor and the second interconnect section respectively.

By taking the inverse Laplace transform of equation (4.37), the time domain response of the RIN section for different load capacitance values is determined and plotted for a step input. 50% time delay (t_d) between the input and output signal is measured from the transient response plot.

The mathematical equivalent model of the RIN section is validated by comparing with the SPICE simulations and the data is tabulated in table 4.1. From the third and fourth columns of table 4.1, it is found that average error between the mathematical model and the SPICE simulations is less than 2%. This shows that the mathematical equivalent model of the RIN section developed using state space approach is closely matching with the SPICE simulations. Comparison of signal delay values of the RIN employing active inductor (our design) with that of passive inductor (work presented in (Rosenfeld and Friedman, 2009)) is given in the fourth and fifth columns of Table 4.1. It can be seen that, that on an average, the delay is reduced by around 24% in a long interconnect network employing an active inductor as the resonating element.

Table 4.1: Delay comparison in the RIN section employing active and passive inductors

Serial No.	Load Capacitance C_L (fF)	Delay using Mathematical Equivalent RIN Model (ps)	Delay using Active Inductor (ps)	Delay using Passive Inductor† (ps)
1	10	245	250	312
2	50	256	260	319
3	100	260	265	326
4	200	265	270	340
5	250	269	273	348.6

†(Rosenfeld and Friedman, 2009)

Usually passive inductors are fabricated in square, hexagonal, octagonal or circular shapes. The physical structure of the fabricated on-chip passive inductor has several turns and several parasitic elements associated with this structure. These parasitic components cause additional delay effect on the propagating signals. In case of active inductors, even the gate capacitances associated with the transistors are used as the capacitors to form the gyrator-C configuration. Hence the stray component effects associated with active inductor differential configuration circuit are very less when compared with the passive inductor structure.

4.4.3 Power Consumption in RIN Section employing Active Inductor

Unlike the passive inductor, active inductor consumes power to generate inductive impedance. However, higher Q would result in lower power consumption which leads to reduced losses (Mukhopadhyay *et al.*, 2006). Results in Table 4.2 support this.

4.4.4 Process Variation Effects on Signal Delay

At deep sub-micron scales, process variations will have significant impact on circuit as well as on metal line characteristics. This is true for active inductor configuration and interconnect line as well. To find the amount of delay variation and output voltage

Table 4.2: Power consumption comparison between RIN section employing passive and active inductor

Inductance (nH)	Passive Inductor (mW)	Active Inductor (mW)
14	6.67	6.50
8	8.25	7.36
7.5	8.42	7.26
6	8.65	7.77
5	9	8.08
1	9.8	8.47

fluctuation due to process and mismatch variations in active inductor and interconnect parameters, Monte Carlo simulations are carried out for 5000 iterations. From figures 4.25 and 4.26, it is observed that interconnect delay variation is insignificant (0.67% for the variation in active inductor circuit and 0.8% for the changes in the interconnect parameters). Further, the output voltage is found to fluctuate less than 0.5% during the ON period and less than 6% during the OFF period of the output signal.

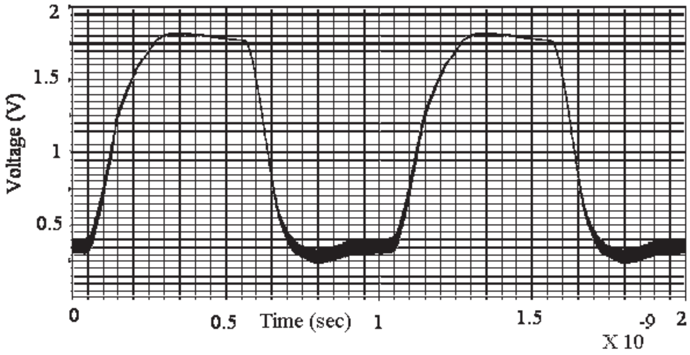


Figure 4.25: Monte Carlo simulation of active inductor with process variations

4.4.5 Area Comparison between Passive Inductor and Active Inductor

Table 4.3 gives the comparison of the approximate area required for the fabrication of passive inductor and the active inductor for different inductance values. From table 4.3,

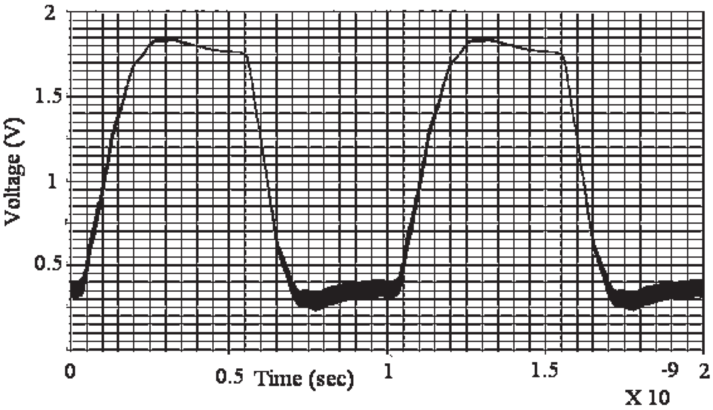


Figure 4.26: Monte Carlo simulation of interconnect with process variations

it is observed that the silicon area required to fabricate an inductance of 7.5 *nH* in the active configuration is roughly 24 times less compared to passive inductor implementation. The physical dimensions of passive inductor is directly related to the desired inductance value and it increases with increasing inductance. Whereas the area of an active inductor marginally increases with increase in inductance value as seen from table 4.3.

Table 4.3: Area comparison for passive and active inductor

Inductance (*nH*)	Inductance type		Reduction in Area
	Approximate area for Passive inductance (μm^2)	Approximate area for Active inductance (μm^2)	
4	1600	182	9×
5.5	3025	196	15×
7.5	5329	224	24×
12	12689	252	50×

4.5 Crosstalk Analysis

The electric and magnetic field energy gets coupled to nearby conductors when the signals travel through interconnect lines. Signals get coupled to adjacent lines due to the mutual inductances (M) and coupling capacitances (CC) between the lines and induce noise in these lines. The strength of the induced noise is dependent on the magnitude of the mutual inductances and the coupling capacitances. Figure 4.27 shows two coupled RIN sections employing active inductors as the resonating elements. In figure 4.27, mutual inductances and coupling capacitances of i^{th} RLGC sections of Line 1 and Line 2 are represented by M_{1i}, CC_{1i}, M_{2i} and CC_{2i} respectively.

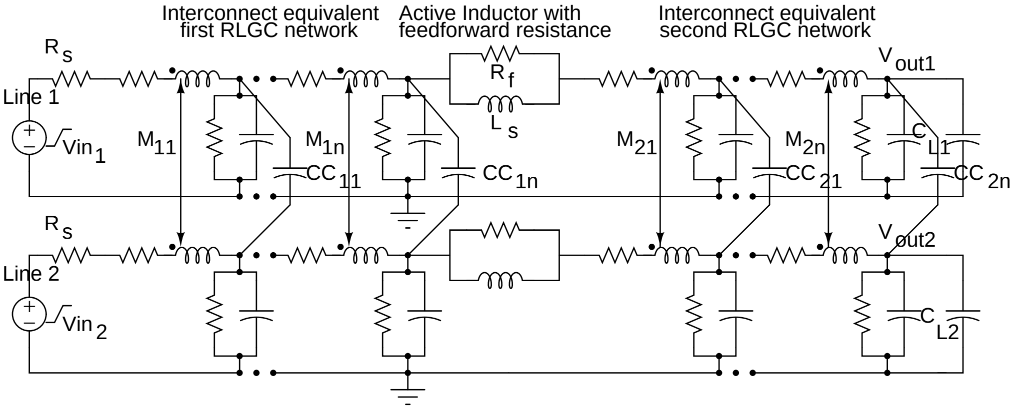


Figure 4.27: Coupled RIN sections employing active inductors

4.5.1 Crosstalk Noise Voltage Analysis in Coupled RIN Sections

Assuming Line 1 as aggressor and Line 2 as victim line, figure 4.27 is used to analyze the amount of noise coupled to the victim line of the RIN section. Figure 4.28 shows the coupled noise voltage waveform in the victim line (at node V_{out2}) of figure 4.27 for the two cases, one with an active inductor and the other with passive inductor as the resonating element. From figure 4.28, it is observed that the far end coupling noise voltage in the victim line is 55% less in the active inductor case compared to the passive inductor case (Case 1 in table 4.4).

To analyze the behavior of the coupled interconnect lines employing active inductors for different input switching conditions, three interconnect lines with coupling effects between the adjacent lines are considered. Coupled noise voltage on the victim line for aggressor - victim - aggressor configuration for the two cases (active inductor and passive inductor as resonating element) under different switching conditions is given in table 4.4. In table 4.4, V_1, V_2 and V_3 indicate the input signal sources for the three interconnect lines. It can be seen that the coupled noise voltage is considerably lower

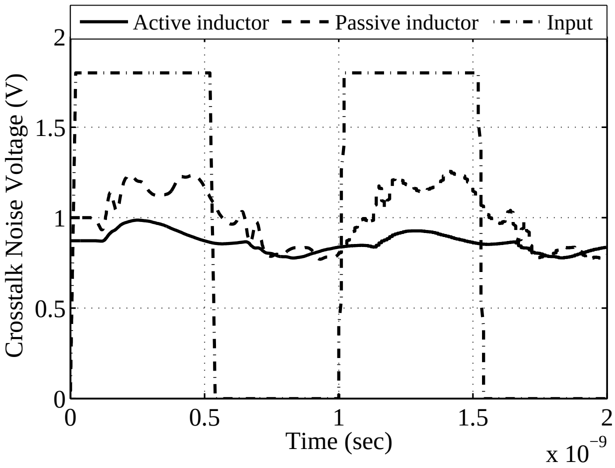


Figure 4.28: Crosstalk noise voltage in the victim line of the coupled RIN sections employing passive and active inductors

in the case of RIN section employing active inductors.

Table 4.4: Coupled noise voltage for different switching conditions

Case	V_1(V) (Aggressor)	V_2(V) (Victim)	V_3 (Aggressor)	V_{c1}^1 (V)	V_{c2}^2 (V)	Reduction in Noise Voltage in %
1	$\uparrow^3$	$-^4$	$\uparrow$	0.38	0.85	55.29
2	$\uparrow$	$\downarrow^5$	$\uparrow$	0.20	1.7	88
3	$\uparrow$	$\downarrow$	$\downarrow$	0.38	1.85	79.45

V_{c1}^1 : Coupled noise voltage with active inductor
V_{c2}^2 : Coupled noise voltage with passive inductor
$\uparrow^3$: Logical 0 to 1 transition
$-^4$: Connected to ground
$\downarrow^5$: Logical 1 to 0 transition

Energy between the two neighboring transmission lines gets coupled due to electric and magnetic field interactions. Passive inductors are fabricated in the form of spiral, hexagonal or circular shapes. Proper current return paths do not exist in these structures. Also due to the form of structures and associated stray components, coupling of energy from the laid out structure to the neighboring lines is high. In contrast to this, active inductor is implemented using MOSFETs with fewer stray components and providing proper current return paths. Hence there is a lesser possibility of energy being coupled from the active inductor configuration to the neighboring lines. These factors reduce the far end noise voltage on the victim line in the coupled resonant interconnect lines with active inductors.

4.6 Conclusions

Mathematical model for a RIN section employing active inductor as the resonating element is derived based on transmission line theory using state space approach. It is observed from the simulation results that an average delay reduction by 24% can be achieved by replacing a passive inductor by an active inductor in the RIN section. The silicon area required to fabricate an active inductor of 7.5 *nH* is approximately 24 times less than that of a passive inductor. Monte Carlo simulations show that the change in the interconnect delay behavior for the process and mismatch variations in the active inductor circuit and interconnect parameters is only 1%. The output voltage fluctuation is less than 0.5% during the high state and 6% during the low state of the output signal. It is also shown that, for different input switching conditions, the far end coupled noise voltage in the victim line is considerably reduced when active inductors are used in place of passive inductors as the resonating element in RIN sections. Further, since clock signals switch continuously, this scheme can be effectively used for reducing the latency/skew of clock signals when transmitted over long nets.

CHAPTER 5

Minimization of Via-Induced Signal Reflection in On-Chip High Speed Interconnect Lines

5.1 Introduction

Present IC technology advancements are allowing data rates exceeding 1 Gbps and this trend will continue to increase with scaling (Tanaka *et al.*, 2002). As previously reported, at these frequencies, the performance of high-speed integrated circuits is increasingly determined by the interconnects. Signal delay, crosstalk, power-supply distribution noise etc. are some of the major signal integrity issues affecting the overall performance of the IC chips and the mitigation of these effects are addressed by many researchers in the past. However, signal reflection due to the impedance discontinuities along the interconnects is a problem that is less addressed in the past. One of the prominent impacts of signal integrity effect is false signal switching leading to performance degradation.

Interconnects behave as transmission lines in GHz regime. When the geometry of the interconnects is altered along the signal path, signal reflections will occur due to impedance mismatch. Changes in the geometry along the path of the interconnects are very common. Some of the examples for impedance discontinuities are connector junctions, wire terminations, vias, etc. Vias are very commonly used structures to connect different metal interconnect layers and become one of the main disruptor of impedance continuity (Laermans *et al.*, 2002). Impedance control along the interconnect path is one of the ways to reduce the signal integrity effects when the signals are sent at high frequencies, typically more than 1 Gbps.

Unlike local interconnects, intermediate and global interconnects have a greater reach across the IC and distribute signals to different parts of the circuit that are geometrically apart. These wires invariably use vias to deliver the signals to the local interconnects and to the devices. The impedance discontinuity at the junction of on-chip intermediate/global interconnect and via result in signal reflections and contributes to the loss of signal. To decrease the signal deterioration, designers try to eliminate impedance mismatch along the signal path. Further, improper connection of the vias between the two metal layers would create considerable voltage breakdown, signal attenuation, crosstalk, switching noise, etc. (Chen *et al.*, 2003).

Via length is negligibly small compared to the signal wavelength at lower frequencies and hence traditionally they are either completely neglected or modeled as a combination of lumped circuit elements such as series inductors and shunt capacitors for ease of circuit analysis. With increasing clock and data rates, parasitics of via cannot be neglected and need to be modeled as RLC structures for accurate analysis. Further, as the technology node decreases due to scaling, via resistance increases significantly and starts contributing to the signal integrity problems (Sicard and Bendhia, 2007).

Several papers analyzing different via structures and their impact on the interconnect performance have been published ((Gu *et al.*, 2002), (Quine *et al.*, 2002),(Maeda *et al.*, 2002)). Capacitance of the vias are extracted either from the solution of integro-differential equations (Kok and De Zutter, 2002) or from full-wave simulations (Onojima *et al.*, 2002). Multiple via interconnect structures have been analyzed by decomposing the geometry into exterior and interior structures (Huang *et al.*, 2005). Efficient modeling methods of multiple vias in high-speed interconnect lines are discussed in (Wu and Tsang, 2009) and (Liu *et al.*, 2009). Further, significant work related to vias has been carried out on impact of differential vias on high-speed design (Xu *et al.*, 2009), modeling differential vias (Simonovich *et al.*, 2009), electrical modeling of 3D vias (Savidis and Friedman, 2008), analysis of crosstalk between non-parallel coupled lines connected with vias in a 4-layer PCB (Han and Park, 2006), Through-Silicon Vias (TSV) (Lau, 2011) etc.

A comprehensive study of the impacts of various via design parameters using full-wave electromagnetic simulator is carried out in (Chang *et al.*, 2007). The design parameters include via diameter, height and length used in a multilayer Printed Circuit Board (PCB). Signal reflections in the interconnect will be minimum for optimized via dimensions. In (Hsu *et al.*, 2008), a artificial neural network approach for the efficient design of reflection-less via structure is presented. In this paper, full-wave analysis is employed to characterize the via structures from which the empirical representation is derived using a neural network method with the physical parameters as inputs and the electrical characterization as the output. With accurate and fast neural network models for the desired via structures, solution space for the feasible geometries of minimum reflection noise can be easily determined.

When a high-speed signal transits through a via that penetrates a plane, parallel-plane resonances are created and introduce extra insertion loss in the transmitting signals. To eliminate via-plane coupling effects, additional ground vias are placed near the signal vias (Wu *et al.*, 2008). But, additional resonance effects will be introduced by the new ground vias. This problem is eliminated by reducing the spacing between the signal vias and ground vias. Further, efforts are made to predetermine the characteristic impedance of multi-layered through-hole vias by choosing appropriate geometrical parameters, dielectric property and placement of ground vias based on semi-analytical scattering model (Gu *et al.*, 2008).

Alternatively, signal reflections can be reduced by altering the shape and structure of the interconnects (Kwon *et al.*, 2003). In (Kim *et al.*, 2005), four types of vias namely staggered, stacked, coaxial and through via are analyzed for their effects on signal reflection and bandwidth.

In most of the work presented in the previous literatures, signal reflection along the interconnects is reduced through the modification of via structure and is mainly aimed towards PCBs. Further, in these cases the structure (geometry) of the vias once fabricated remains fixed and modification of via geometry is not feasible to suit newer frequencies of operation.

In this work, via-induced signal reflection reduction in ICs is addressed by incorporating a simpler technique where-in an additional capacitance is included at the interconnect-via junction for impedance matching. This method does not require any modification to the technology specific interconnect geometry. Via impedance is calculated from its equivalent circuit and the effect of impedance mismatch on signal reflections at the junction of the metal interconnect line and the via is analyzed for two types of models: (i) two adjacent interconnect metal layers connected through a single via (2-layer model) and (ii) multi-level interconnects (layer 6 to layer 1) connected through five vias (6-layer model). This method can be extended to interconnect layers connected through any arbitrary number of vias. Further, the method is amenable to frequency tunability by making use of a digitally switchable bank of capacitors in place of the single matching capacitor at the interconnect-via junction.

5.2 Vias

Via is a small conductive cylindrical hole drilled from one layer to another layer and used to connect different interconnect levels in an IC. Via structure consists of a barrel, a pad and an anti-pad as shown in figure 5.1 (Hall *et al.*, 2000). Via barrel is a conductive material that fills the hole to allow an electrical connection between the connected layers. Via pad connects the barrel to the component or trace while antipad is a clearance hole between the pad and the metal on a layer to which no connection is required.

In DSM regime, via effects are significant and cannot be neglected. In (Katti *et al.*, 2009), via resistance (R_{via}), inductance (L_{via}) and capacitance (C_{via}) are modeled as a function of physical dimensions and material characteristics. An equivalent lumped RLC model represented in the form of T network is shown in figure 5.2. The resistance, inductance and capacitance values of the via are given by,

$$R_{via} = \frac{\rho l_{via}}{\pi r_{via}^2} \tag{5.1}$$

$$L_{via} = \frac{\mu_0}{4\pi}\left[l_{via} ln\left(\frac{2l_{via} + \sqrt{r_{via}^2 + (2l_{via})^2}}{r_{via}}\right) + \left(r_{via} - \sqrt{r_{via}^2 + (2l_{via})^2}\right)\right] \tag{5.2}$$

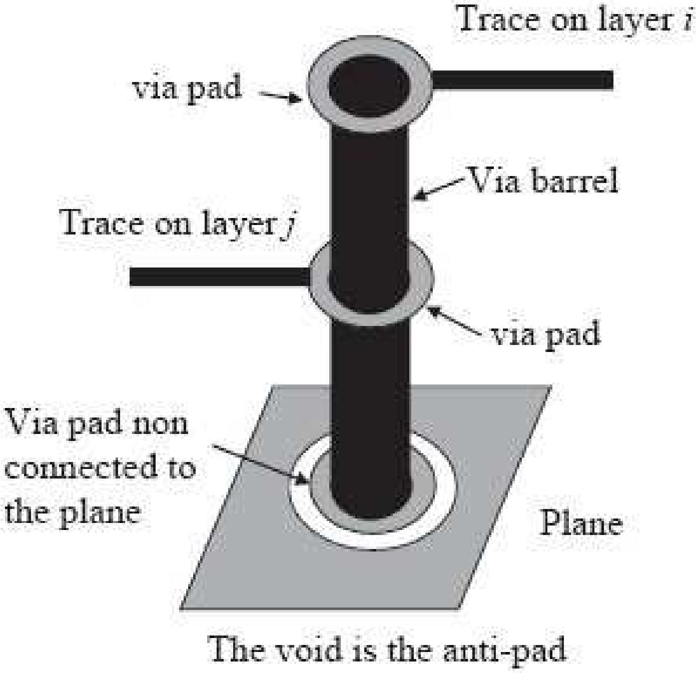


Figure 5.1: Via structure

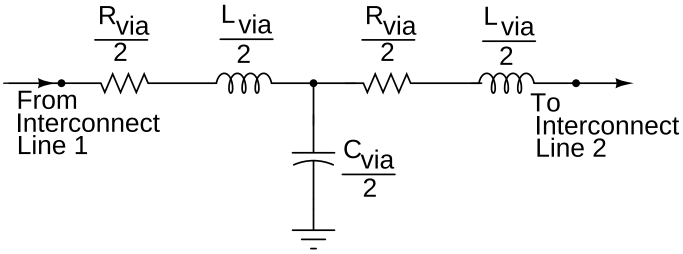


Figure 5.2: Lumped RLC equivalent via model

$$C_{via} = \frac{2\pi\varepsilon_r\varepsilon_0 l_{via}}{ln((r_{via}+t_{via})/r_{via})} \tag{5.3}$$

where ρ, r_{via}, l_{via}, and t_{via} denote resistivity of the conducting material, radius, length and dielectric thickness around the via respectively. The values of R_{via}, L_{via} and C_{via} for 65-nm technology node are computed using equations (5.1) to (5.3) and are found to be equal to 3.5 Ω, 26.09 pH and 113.98 fF respectively.

For contemporary through silicon via architectures, the inductive voltage drop is found to exceed resistive voltage drop for frequencies above 1 GHz and hence the via structure can be assumed to behave predominantly as an inductive load.

5.3 Impedance Matching at Interconnect-Via Junction

Figure 5.3 shows the model of two metal interconnect layers (L_1 and L_2) connected through a single via. At high signal frequencies, interconnects behave as transmission lines and electric signals propagate as electromagnetic waves. When these waves propagate through the interconnect-via structure of different characteristic impedance regions two things happen: (i) A portion of the wave is reflected back from the impedance discontinuity region to the source-end and (ii) A portion of the wave is transmitted through the via. The simultaneous existence of both the transmitted and reflected waves are direct result of the boundary conditions that must be satisfied when solving Maxwells equations at the interface between the two regions.

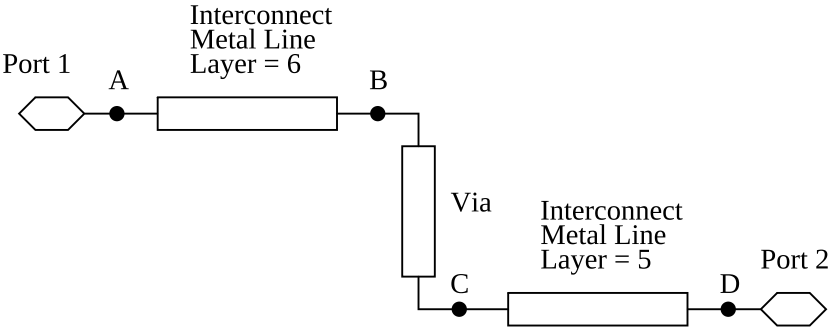


Figure 5.3: Model of the two interconnect layers connected through a via

When an electromagnetic wave is propagating in the transverse mode, difference of the incident and reflected waves must equal to the transmitted wave, i.e.

$$v_t = v_i - v_r \tag{5.4}$$

$$\frac{i_t}{Z_{via}} = \frac{i_i}{Z_0} - \frac{i_r}{Z_0} \tag{5.5}$$

where v_i, v_r, v_t, i_i, i_r and i_t indicate the incident, reflected and transmitted voltage and current waves respectively. The parameters Z_0 and Z_{via} denote the characteristic impedance of the transmission line and impedance of the via respectively. Since the incident waves are known, equations (5.4) and (5.5) are solved simultaneously for the transmitted and reflected portions of the wave. Thus, v_t and v_r are given by,

$$v_t = v_i \frac{2Z_{via}}{Z_{via} + Z_0} \tag{5.6}$$

$$v_r = v_i \frac{Z_{via} - Z_0}{Z_{via} + Z_0} \tag{5.7}$$

The reflection coefficient (Γ) is a measure of how much of the signal is reflected back by the intersection between the two impedance regions and the transmission coefficient (ξ) represents how much of the signal is transmitted. From equations (5.6) and (5.7), Γ and ξ are given by

$$\Gamma = \frac{v_r}{v_i} = \frac{Z_{via} - Z_0}{Z_{via} + Z_0} \tag{5.8}$$

$$\xi = \frac{v_t}{v_i} = \frac{2Z_{via}}{Z_{via} + Z_0} \tag{5.9}$$

When the behavior of the interconnect is approximated to that of a transmission line at high frequencies, the characteristic impedance is given by (Hall and Heck, 2009).

$$Z_0 = \sqrt{\frac{\varepsilon_0 \mu_0}{\varepsilon_{eff}}} \frac{1}{C_a} \tag{5.10}$$

where

$$C_a = \begin{cases} \dfrac{2\pi\varepsilon_0}{ln(8h/w_e + w_e/4h)} & , \dfrac{w_e}{h} \leq 1 \\ \varepsilon_0 [\dfrac{w_e}{h} + 1.393 + 0.667 ln(\dfrac{w_e}{h} + 1.444)] & , \dfrac{w_e}{h} > 1 \end{cases} \tag{5.11}$$

$$\varepsilon_{eff} = [\frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}(1 + 12\frac{h}{w_e})^{-1/2}] \tag{5.12}$$

$$w_e = \begin{cases} w + 0.398t(1 + ln\dfrac{4\pi w}{t}) & , \dfrac{w}{h} \leq \dfrac{1}{2\pi} \\ w + 0.398t(1 + ln\dfrac{2h}{t}) & , \dfrac{w}{h} > \dfrac{1}{2\pi} \end{cases} \tag{5.13}$$

In equation (5.10), C_a and ε_{eff} indicate the distributed capacitance of the microstrip line and the effective dielectric constant of the substrate material respectively. These parameters are given in equations (5.11) and (5.12). The identifiers w, t denote the width and thickness of the interconnect, h and w_e denote the substrate thickness and effective width of the interconnect that accounts for the extra capacitance caused by the finite thickness of the signal conductor respectively. This is so because the electric field will also be established between the edges of the conductor and the reference plane for thicker signal conductors resulting in increased capacitance. Hence, w_e is slightly wider than w to account for the extra capacitance.

5.3.1 Determination of Matching Capacitance (C_m)

In section 5.2, it is shown that at 65 *nm* technology node and for frequencies above 1 GHz, the vias predominantly behave as inductive load. To compensate this impedance, the optimal way is to connect a capacitive load at the junction of the interconnect and the via. Figure 5.4 shows the proposed method used to reduce the signal reflection in the two layer model in-which a matching capacitive load (C_m) is added at the interconnect-via junction. The input impedance (Z_{in}) seen from the right terminal of the first interconnect layer (point B in figure 5.3) is computed by replacing the via by its equivalent circuit given in figure 5.2. Expression for Z_{in} is given by,

$$Z_{in} = \left(\frac{R_{via} + j\omega L_{via}}{2}\right) + \left[\frac{1}{j\omega C_{via}} \parallel \left(\frac{R_{via} + j\omega L_{via}}{2} + Z_{02} + (\frac{1}{j\omega C_L} \parallel Z_{t2})\right)\right] \quad (5.14)$$

where Z_{02}, Z_{t2} and C_L indicate the characteristic impedance of the second interconnect layer, terminating resistance used for S parameter analysis at the input and output side of the structure (figure 5.5) and load capacitance respectively.

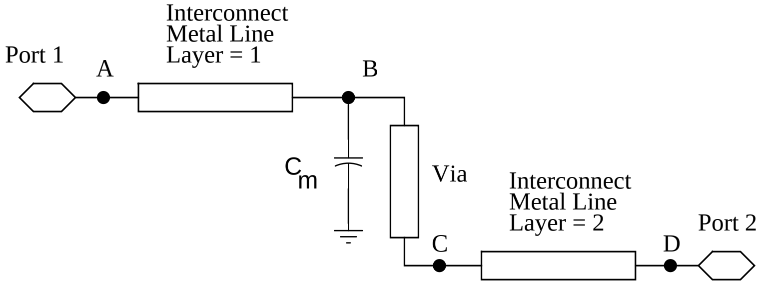


Figure 5.4: Proposed method to reduce signal reflection in two-layer model

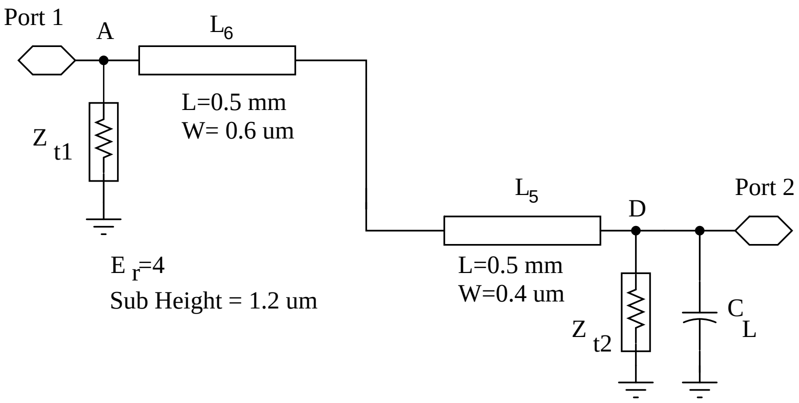


Figure 5.5: Model of two directly connected interconnect layers

Simplifying equation (5.14) results in

$$Z_{in} = x + \cfrac{1}{j\omega C_{via} + \cfrac{1}{x + Z_{02} + \cfrac{Z_{t2}}{j\omega C_L Z_{t2} + 1}}} \tag{5.15}$$

where

$$x = \frac{R_{via} + j\omega L_{via}}{2}$$

Signal reflection is minimum when the characteristic impedance of the microstrip line matches with the via impedance. In such a scenario, matching between the interconnect and the via can be easily achieved by connecting an appropriate matching capacitance between point B and ground as in figure 5.4. If Z_{01} represents the characteristic impedance of the interconnect between points A and B in figure 5.4, then we can achieve zero reflection at the interconnect-via junction provided an impedance seen at point B (Z_{match}) matches with Z_{01}. That is to say,

$$Z_{01} = Z_{match} = \left(\frac{1}{j\omega C_m} \parallel Z_{in}\right) \tag{5.16}$$

Substituting the expression for Z_{in} in equation (5.16) and solving for C_m, we get,

$$C_m = \frac{1}{jw}\left[\frac{1}{Z_{01}} - \cfrac{1}{x + \cfrac{(a+jb)}{(c+jd+1)}}\right] \tag{5.17}$$

where

$$
\begin{aligned}
x &= \frac{R_{via} + j\omega L_{via}}{2} \\
a &= R_{via} - \omega^2 L_{via} C_{via} Z_{t2} + 2Z_{02} + 2Z_{t2} \\
b &= R_{via} C_L Z_{t2} + L_{via} + 2Z_{02} C_L Z_{t2} \\
c &= -\omega^2 C_{via} (R_{via} C_L Z_{t2} + L_{via} + 2Z_{02} C_L Z_{t2}) \\
d &= \omega C_{via} (R_{via} - \omega^2 L_{via} C_L Z_{t2} + 2Z_{02} + 2Z_{t2})
\end{aligned}
$$

The value of C_m is adjusted for minimum signal reflection (maximum impedance matching) for a given operating frequency.

5.4 Signal Reflection Reduction in a Two-Layer Interconnect Structure

Two-layer and six-layer interconnect models are designed and simulated using Advanced Digital System (ADS) software. S-parameter analysis is used to analyze the signal reflection at the input and output side of the model. Interconnect parameters of 65-nm technology node are used in the simulations and are listed in Table 5.1 (Bai *et al.*, 2005).

Table 5.1: Interconnect layer thickness, width and spacing

Layer	Thickness (μm)	Width (μm)	spacing (μm)
Metal 1	0.20	0.13	0.10
Metal 2	0.25	0.15	0.10
Metal 3	0.30	0.17	0.10
Metal 4	0.50	0.28	0.05
Metal 5	0.80	0.40	0.05
Metal 6	1.20	0.60	0.02

Figures 5.5 and 5.6 shows the interconnection of metal 5 and metal 6 layers (refer table 5.1 for layer parameters) without and with via arrangement used for S-parameter analysis. In figure 5.6, following via dimensions are considered: via diameter of 0.4 μm, pad diameter of 0.65 μm, via height of 0.4 μm and dielectric thickness 1 μm. In the simulations, the values of the metal length, load capacitance C_L, terminating resistances Z_{t1} and Z_{t2} are considered to be 0.5 mm, 0.25 pF, 76 Ω and 88 Ω, respectively.

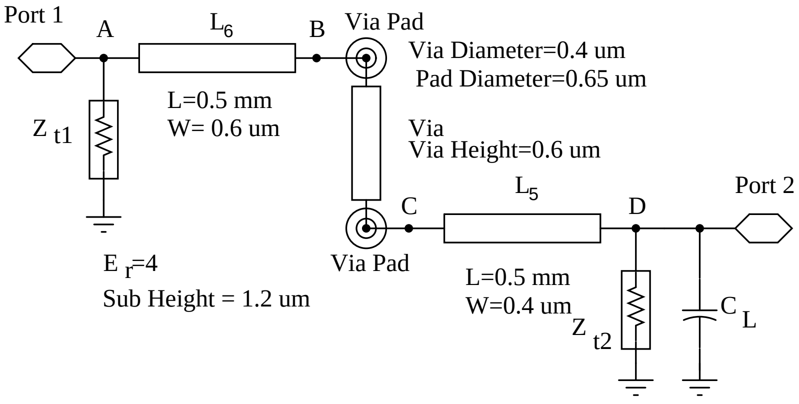


Figure 5.6: Model of two interconnect layers connected through a via

The effect of via on signal reflection can be seen by comparing the S-parameter analysis of two-layer interconnect structures - one in which the metal layers are directly connected as in figure 5.5 (not practical in real scenario) and the other through a via (as in figure 5.6). Figure 5.7 shows the signal reflection (parameter S_{11}) measured at point A in figures 5.5 and 5.6. From figure 5.7, it can be seen that up to a frequency of 10 GHz, there is a significant increase in the signal reflection in the structure employing via in comparison to the structure without a via. This is due to the impedance mismatch between the interconnect layer and the via.

An equivalent of the via lumped RLC model represented in the form of **T** network is shown in figure 5.2. Figure 5.8 shows the input signal reflection at point A in figure 5.6 with via and its equivalent model. Results show that both the responses are closely matching. Hence the model shown in figure 5.2 can be used as the equivalent of the via. The arrangement to mitigate the signal reflection at the junction of the interconnect and the via is shown in figure 5.9. Figure 5.10 shows the signal reflections at the input side (point A in figure 5.9) for different capacitance (C_m) values.

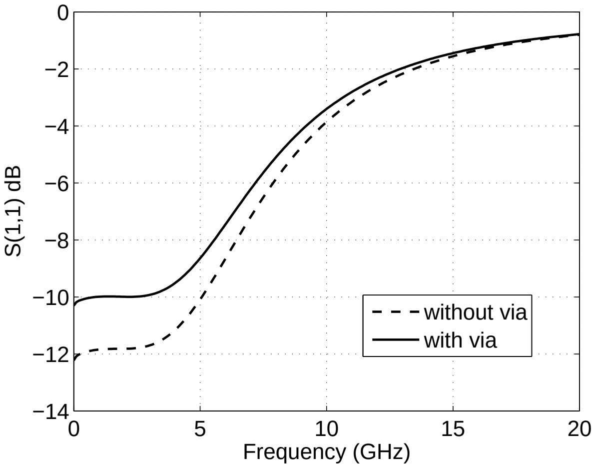


Figure 5.7: Signal reflections with and without via

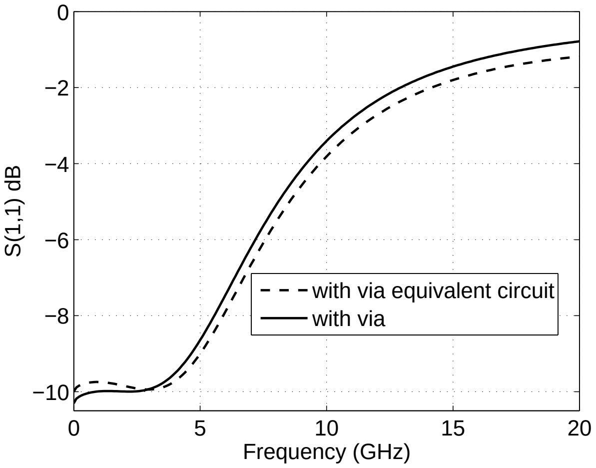


Figure 5.8: Comparison of signal reflections with via and its equivalent model

It is observed that the minimum signal reflection point is dependent the matching capacitance C_m. In this work, we are interested to have low signal reflections in the range 1-10 GHz. By keeping the minimum signal reflection point at 5 GHz, the theoretical value of C_m (Equation (5.17)) is found to be 345 fF. From the simulations, the matching capacitance value is found to be 335 fF at 5 GHz (figure 5.10), which is in close agreement with the theoretical value.

Figures 5.11 and 5.12 show the signal reflection (S_{11}) and transmission loss (S_{21}) at point A with and without matching capacitance (at point B in figure 5.9). From figure 5.11, it can be seen that there is a clear advantage in using a matching capacitance

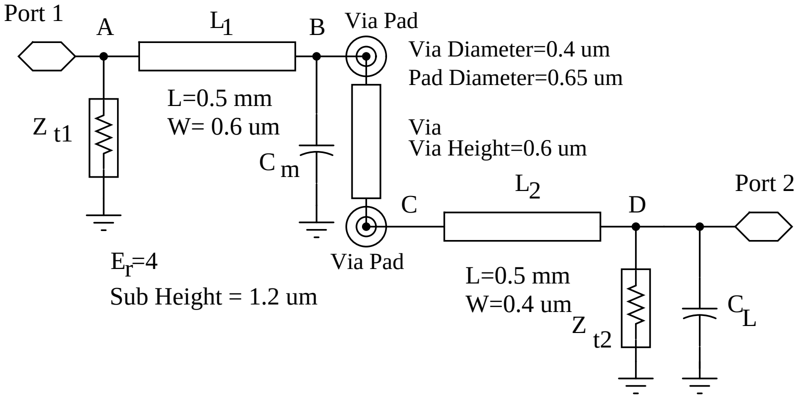


Figure 5.9: Proposed method to reduce signal reflection at the interconnect-via junction

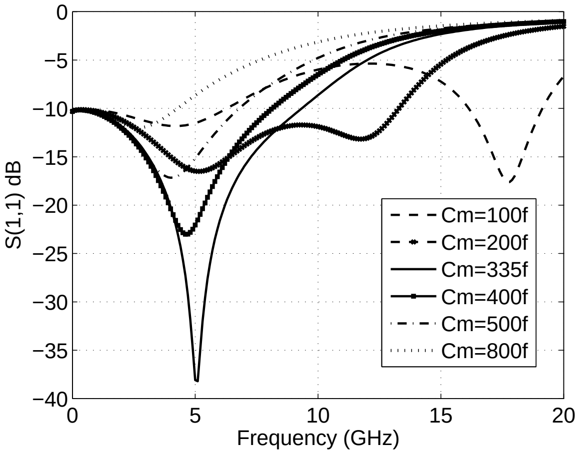


Figure 5.10: Signal reflection for different matching capacitance values

to reduce signal reflections.

5.4.1 Signal Reflection Reduction in Six-Layer Structure

Analysis of the proposed method is carried out for a six-layer interconnect structure in which the two interconnect metal lines, viz., layer 6 and layer 1 are connected through five vias (Kim *et al.*, 2005). The ADS setup for creating six-layer structure is given in figure 5.13. The values of the relative dielectric constant of the substrate (ε_r[n]), height of substrate (H[n]), dielectric loss tangent (TanD[n]), metal thickness (T[n]), conductivity (Cond[n]) and type of the metal layer (LayerType[n]) are listed in figure 5.13.

Capacitances are added at the junctions of each interconnect layer and the via. The

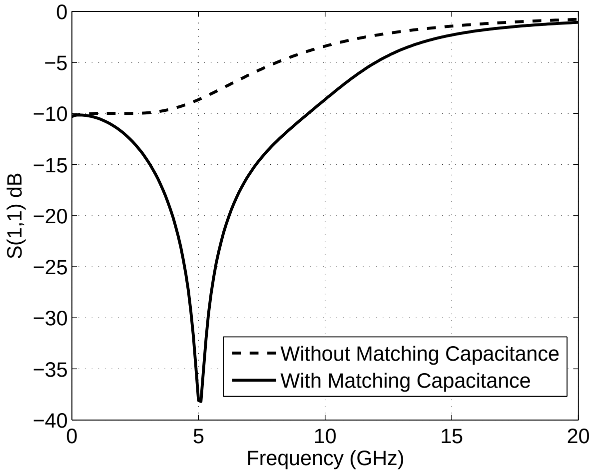


Figure 5.11: Signal reflection with and without capacitance in the two-layer interconnect model

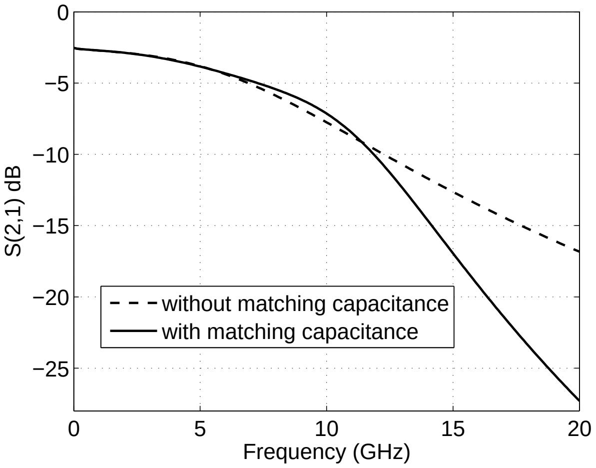
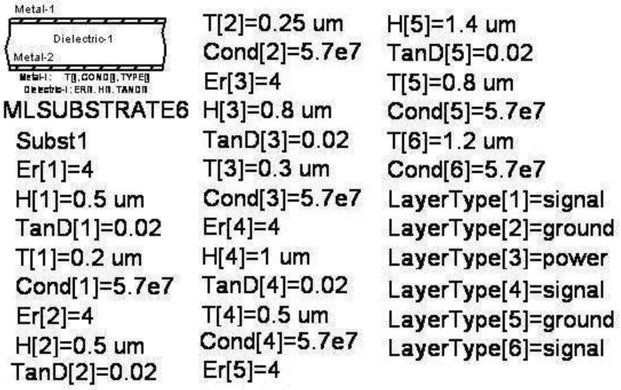


Figure 5.12: Transmission loss with and without capacitance in the two-layer interconnect model

arrangement for the connection of two interconnect lines from layer 6 to layer 1 through vias is shown in figure 5.14. Vias are connected with suitable dimensions which are matching with the width of the corresponding interconnect layers.

Figures 5.15 and 5.16 show the signal reflection and the transmission loss with and without capacitances in a six-layer structure. It can be seen that, there is significant improvement in signal reflection and transmission loss with the addition of the matching capacitances.

Using the proposed method, signal reflections can be reduced in a multi-layer struc-



MLSUBSTRATE6
Subst1
Er[1]=4
H[1]=0.5 um
TanD[1]=0.02
T[1]=0.2 um
Cond[1]=5.7e7
Er[2]=4
H[2]=0.5 um
TanD[2]=0.02
T[2]=0.25 um
Cond[2]=5.7e7
Er[3]=4
H[3]=0.8 um
TanD[3]=0.02
T[3]=0.3 um
Cond[3]=5.7e7
Er[4]=4
H[4]=1 um
TanD[4]=0.02
T[4]=0.5 um
Cond[4]=5.7e7
Er[5]=4
H[5]=1.4 um
TanD[5]=0.02
T[5]=0.8 um
Cond[5]=5.7e7
T[6]=1.2 um
Cond[6]=5.7e7
LayerType[1]=signal
LayerType[2]=ground
LayerType[3]=power
LayerType[4]=signal
LayerType[5]=ground
LayerType[6]=signal

Figure 5.13: Setup for the simulation of six-layer structure

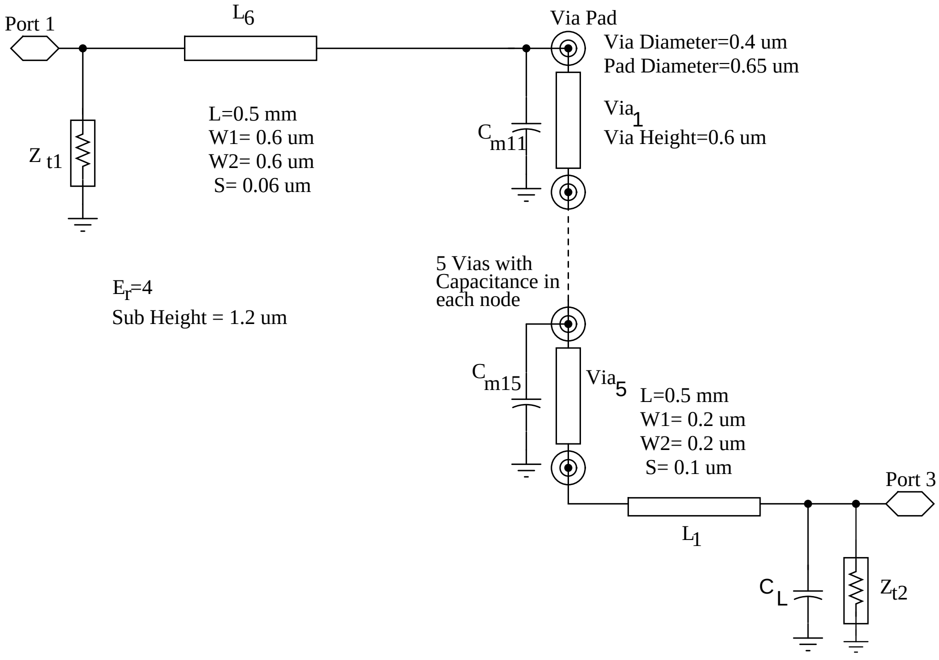


Figure 5.14: Layer 6 to layer 1 through five vias with matching capacitances

ture. In such structures, signal lines are surrounded by ground/power lines for reducing crosstalk. Hence the matching capacitances can be easily connected between the ground plane and the junction of the interconnect layer and the via. The matching capacitances (C_m) can be realized using MIM capacitors (Ng *et al.*, 2005). Since the value of C_m is moderate, the area consumed by these capacitors will not be very significant.

RF and mixed-signal integrated circuits employ capacitor elements for decoupling, filtering etc. Metal-Insulator-Metal (MIM) capacitor is one of the widely used methods in these applications which has high conductive electrodes and low parasitic capaci-

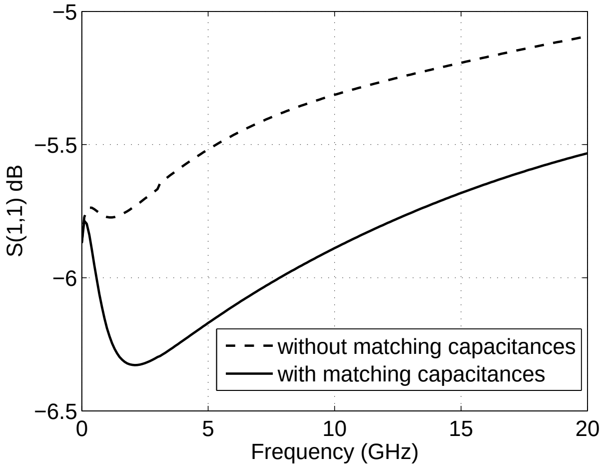


Figure 5.15: Signal reflection with and without the capacitances in the six-layer structure

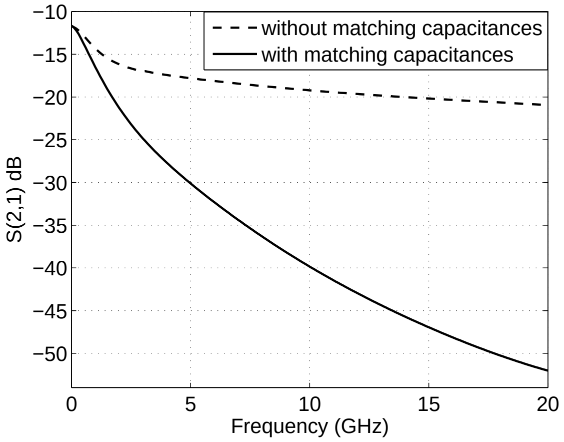


Figure 5.16: Transmission loss with and without the capacitances in the six-layer structure

tances. In MIM capacitors, there is a thin dielectric between a metal layer and a special metal layer called capacitor top metal. The planar MIM capacitor structure offers the advantage of flexibility in inserting it below the top metal layer of a multilevel interconnect structure or between two intermediate metal levels for applications which requires such a design. Typically, capacitance is around $1 fF/\mu m^2$ (at the level below top metal) and varies with different metal levels and line widths. A five-level interconnect structure in which the capacitance is realized between the second (Metal 2) and the third metal level (Metal 3) using an extra metallic layer in order to achieve high capacitance value is shown in figure 5.17(Gruner et al., 2007).

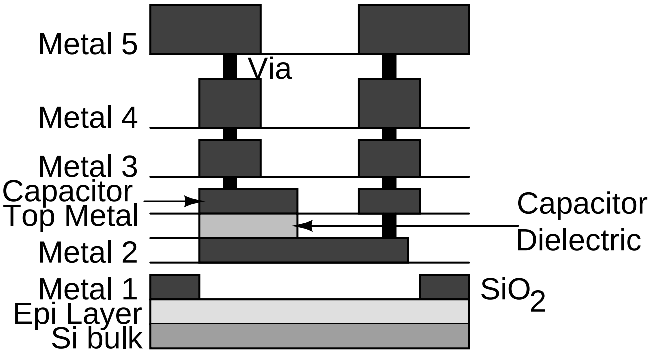


Figure 5.17: MIM capacitor within the stacked metallic layers

5.4.2 Scope for Frequency Tunability

The proposed method can be used to reduce the signal reflection at the junction of the metal interconnect layer and the via for different frequencies of operation. Figure 5.18 shows the arrangement of the frequency-tunable signal reflection reduction for the model of two interconnect layers connected through a via. A bank of capacitors (C_{m1} to C_{mn}) are connected using a set of switches (S_1 to S_n) in place of the matching capacitance at the junction of the metal layer and the via. Depending upon the frequency of operation, digitally controlled switches are turned ON or OFF so as to present right value of capacitance at the interconnect-via junction for impedance matching. Although, parasitic capacitances of the switches need to be taken into account while computing the optimum matching capacitance to minimize signal reflection for a given frequency, the method helps in reducing the reflection for any frequency of operation.

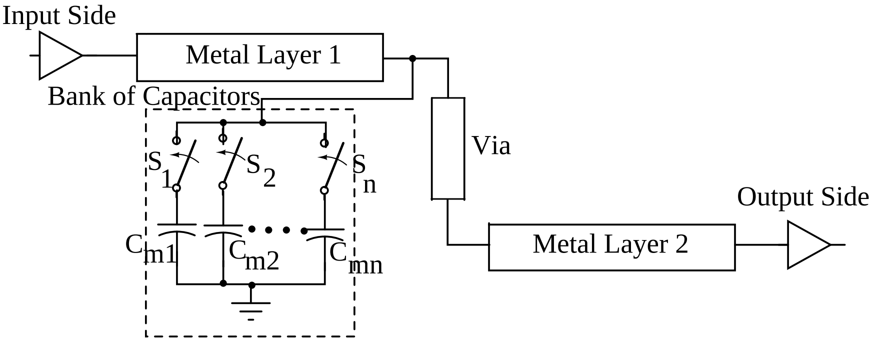


Figure 5.18: Arrangement for the frequency-tunable signal reflection reduction

5.5 Conclusions

S-parameter analysis shows that at high frequencies of operation a portion of the signal gets reflected due to impedance mismatch at the junction of the interconnect and the via. In this work, an arrangement to reduce the signal reflection by adding a matching capacitance at the interconnect-via junction is presented. The matching capacitance value is analytically computed and is found to be in close agreement with the simulation results. In the two-layer interconnect model, signal reflections are reduced to less than -10 dB in the frequency range of 1 to 10 GHz and is below -35 dB at the tuned frequency of 5 GHz. The proposed method is applied to a six-layer interconnect structure and the signal reflection is found to reduce considerably. The above system can be extended to different operating frequencies by incorporating digitally tunable capacitive loading.

CHAPTER 6

Interconnect Delay Reduction in Clock Network using CRLH Metamaterial Structure

6.1 Introduction

Today's high speed ICs have highly complex architectures. Generally, such systems are developed using several sub-blocks, each sub-block performing some specific task. Sub-blocks are connected through metal interconnect lines and clock signals are used for synchronization. Large systems comprise one or more clock domains and generally clocks are routed through top interconnect layers.

With technology scaling, clocks are becoming faster and faster and the impact of clock non-idealities such as latency, skew and jitter become more pronounced in deciding the system performance. Since clock signals being the highest frequency signals in any IC, controlling the clock non-idealities to acceptable levels is a very challenging task. In newer technologies, unless the signals are delivered at the right place at the right time, the benefits of scaling would eventually diminish and limit the maximum speed and efficiency of the IC chips . Hence, there is a need to reduce the clock non-idealites especially in high frequency applications to improve the IC performance. In this work, a method is presented to reduce the latency and skew of clock signals using a resonating network that employ metamaterial structures.

Metamaterials are artificially engineered structures with several interesting properties that are not found in naturally occurring materials. The Left-Handed Metamaterial is first proposed and investigated by the Russian physicist Veselago (Veselago, 1968). He speculated on the possible existence of left handed materials with the characteristics of simultaneous negative permittivity (ε) and permeability (μ) which may lead to the unique electromagnetic properties such as the reversal of Snells law and Doppler effect.

Structures having negative μ and ε can be artificially created and are broadly classified into two types: Resonant (Pendry *et al.*, 1999) and Transmission line ((Lai *et al.*, 2004)). In resonant approach, metamaterials are implemented either by loading the host transmission line with Split Ring Resonators (SRR) (Pendry *et al.*, 1999) or with Complementary Split Ring Resonators (CSRR) (Bonache *et al.*, 2006). In the former case, SRRs provide the negative effective μ to the transmission line whereas the required negative ε is achieved by the presence of shunt wires or vias. In the latter case, CSRRs are responsible for the negative effective ε whereas the negative effective μ is obtained by etching series gaps in the conductor strip. Even though these structures are very exciting, resonant based metamaterials are of little practical interest for engineering applications since these structures are resonant in nature and consequently exhibit high loss and narrow bandwidth.

A Transmission Line (TL) based structure does not suffer from this draw back. A lossless transmission line can be modeled as a distributed LC circuit with a series inductance and a shunt capacitance. In a TL based metamaterial structure, transmission line is periodically loaded with series capacitances and shunt inductances (Lai *et al.*, 2004). Depending upon the dominant passive element among the series and shunt inductances and capacitances, the structure so created exhibits Left Handed (LH) (at lower frequencies) and Right Handed (RH) (at higher frequencies) behavior. Hence, such structures are termed as Composite Right/Left Handed (CRLH) transmission lines (Sanada *et al.*, 2004). Some of the CRLH structures exhibit continuous transition between the backward and forward transmission bands and are said to be balanced. The characteristic impedance of such CRLH structures smoothly varies with frequency in the vicinity of the transition frequency.

One of the advantages of TL metamaterial structure is that they are non-resonant in nature and consequently exhibit low loss and broad bandwidth. Another advantage is that a TL CRLH structure can be engineered in planar configurations and is compatible with modern Microwave Integrated Circuits (MICs).

CRLH metamaterial structures are used in various types of applications especially at microwave frequencies. CRLH structures include guided wave properties such as dual-band operation, bandwidth enhancement, multilayer-architecture super compactness, arbitrary coupling level, zeroth-order resonance etc. Hence, CRLH structures are being used in some typical guided wave applications such as Hybrid Coupler, Wilkinson Power Divider, Hybrid Ring etc. (Caloz and Itoh, 2006). In guided-wave applications, energy remains essentially confined within the structures. However, if a metamaterial structure is open to free space, it supports a fast-wave mode called leaky-wave (LW) mode. In this mode, the structure radiates and can be used as an antenna or as a reflector. Unique radiation effects may be obtained with CRLH structures due to their rich and unusual propagation properties. Some of the typical antennas using CRLH structure include LW antenna, Conical-Beam Antenna, Full-Space Scanning Antenna, Zeroth Order Resonating antenna, Dual-Band CRLH TL Resonating Ring antenna etc. (Caloz and Itoh, 2006).

CRLH as a resonator and its extraordinary resonant characteristics supporting an infinite-wavelength wave at a finite non-zero frequency is discussed in (Sanada *et al.*, 2003). In this paper, it is shown that the resonant frequency of the Zero Order Resonance (ZOR) is independent of the physical length so that the resonator can be arbitrarily small provided that sufficient reactance can be squeezed in a short length. Consequently, the size of a CRLH resonator is very small when compared to the normal resonators at microwave frequencies. Electronically tunable zero order resonator based on CRLH-TLs is given in (Pramod and Vinoy, 2011). Tunability is obtained by use of varactors connected in shunt to the short circuited stub. Also CRLH can be used in a broadband differential phase shifter as one of the differential phase-shift arm instead of the conventional coupled line (Zou *et al.*, 2007).

In some of the microwave applications, CRLH structures are used as delay lines. Delay lines based on microstrip transmission lines show lower loss and wider bandwidth but fail to achieve longer delay owing to high speed RF/microwave signals. CRLH structures are used to overcome these problems at microwave frequencies. In (Abielmona *et al.*, 2007), CRLH transmission line along with two mixers and a low-pass filter provides tunable group delay for impulse and continuous-wave signals. Group delay tunability is possible because of the dispersion property of the CRLH transmission line. Tunable delay is achieved without suffering from the drawbacks of conventional delay lines in terms of matching, frequency of operation and planar circuit implementation. In (Abielmona *et al.*, 2009), CRLH structure is used as Dispersive Delay Line (DDL) to process the signals for analog signal processing applications. CRLH DDL offers advantages such as arbitrary frequency of operation and wide bandwidth, filling a gap with the existing and competitive various DDL technologies (Abielmona *et al.*, 2009). Application of CRLH as Delay Line Discriminator (DLD) is proposed in (Mulagada and Weldon, 2010). DLD is used for the instantaneous frequency measurement and is particularly useful in radar detection systems.

CRLH structures also find applications in microelectronics circuits. In (Sebak *et al.*, 2007), CRLH is cascaded with a power amplifier circuit to minimize the group-delay of the circuit. Such an approach does not alter the original power amplifier circuit characteristics such as gain and return loss. CRLH TL for the design of dual band high efficiency power amplifiers working in Common Emitter (CE) class is presented in (Jimenez-Martin *et al.*, 2009). The harmonic termination can be synthesized using the metamaterial lines and particularly suitable for CE class amplifiers. The nonlinear phase response of the CRLH is utilized to design arbitrary dual-band amplifiers. In another application, two CMOS integrated circuits are presented that utilize CRLH for zero phase insertion (Podilchak *et al.*, 2009).

In addition to the normal CRLH TLs, new structures have been developed that exhibit the characteristics of simultaneous negative ε and μ. Some of the typical structures include Dual Composite Right/Left Handed (D-CRLH) transmission lines (Caloz, 2006), Via-Free Microstrip CRLH (Eberspacher *et al.*, 2009), Reconfigurable metamaterial based CRLH (Wiwatcharagoses and Chahal, 2011) etc. Also CRLH structures are used to realize Bandpass filters (Zhu *et al.*, 2007) and various types of other filters. These filters offer advantages in terms of compact dimensions and low loss.

In the literature, it is found that CRLH structures are widely used as delay lines in various applications. In microwave applications, delay in clock signals when transmitted through metal interconnects is an important issue because at such high frequencies, even a delay of a few pico seconds is detrimental to the proper functioning of the circuit. In this work, it is shown that the delay in the propagation of clock signals in a long interconnect can be considerably reduced by augmenting it with a CRLH metamaterial structure that resonates at the desired clock frequency.

6.2 Theory of RH, LH and CRLH Transmission Lines

6.2.1 RH-TL and LH-TL

Transmission lines have positive ε and μ and are termed as Right-Handed (RH) materials. An infinitely small section of the RH TL is represented by a series inductance and a parallel capacitance as shown in figure 6.1(a). For RH-TLs, phase velocity and the group velocity have positive values.

Transmission line, with a negative phase velocity (but with a positive group velocity) would be useful in some applications. The equivalent circuit of this transmission line will consist of a series capacitance and a parallel inductance and is shown in figure 6.1(b). This type of transmission line does not exist in practice, but a structure can be created which will have these properties.

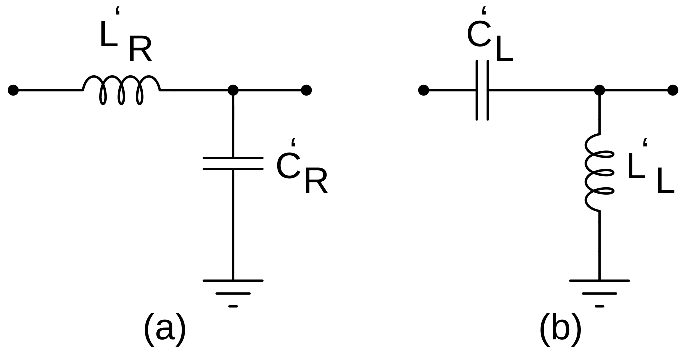


Figure 6.1: Equivalent circuits of (a) RH-TL and (b) LH-TL

In figure 6.1, $L_R^{'}$, $C_R^{'}$, $L_L^{'}$ and $C_L^{'}$ indicate the distributed inductances and capacitances of RH-TL and LH-TL respectively (all values are per unit length). For the equivalent circuits shown in 6.1, expressions to calculate the propagation constant (γ) and the characteristic impedance (Z_0) are given by

$$\gamma = \sqrt{Z'(\omega)Y'(\omega)} = \alpha + j\beta \tag{6.1}$$

$$Z_0 = \sqrt{\frac{Z'(\omega)}{Y'(\omega)}} \tag{6.2}$$

where $Z^{'}(\omega)$ and $Y^{'}(\omega)$ denote the impedance of the series branch and the admittance of the parallel branch respectively. The parameters α and β indicate the attenuation constant and phase constant respectively. If it is assumed that the line is lossless ($\alpha = 0$), then the propagation constant is pure imaginary, while the impedance is pure real. Expression for the impedance and admittance of RH-TL shown in figure 6.1(a) is written as

$$Z^{'}(\omega) = j\omega L_R^{'} \quad and \quad Y^{'}(\omega) = j\omega C_R^{'} \tag{6.3}$$

Substituting equation (6.3) in equations (6.1) and (6.2), we get

$$\beta_{RH-TL} = \omega\sqrt{L_R^{'}C_R^{'}} \quad and \quad Z_{c,RH-TL} = \sqrt{\frac{L_R^{'}}{C_R^{'}}} \tag{6.4}$$

Equation (6.4) indicates that $\beta_{RH-TL} > 0$. Impedance and admittance of LH-TL shown in figure 6.1(b) is written as

$$Z^{'}(\omega) = \frac{1}{j\omega C_L^{'}} \quad and \quad Y^{'}(\omega) = \frac{1}{j\omega L_L^{'}} \tag{6.5}$$

Substituting equation (6.5) in equations (6.1) and (6.2), we get

$$\beta_{LH-TL} = -\frac{1}{\omega\sqrt{L_L^{'}C_L^{'}}} \quad and \quad Z_{c,LH-TL} = \sqrt{\frac{L_L^{'}}{C_L^{'}}} \tag{6.6}$$

Equation (6.6) indicates that $\beta_{LH-TL} < 0$. Equations (6.4) and (6.6) are termed as dispersion equations for RH-TL and LH-TL respectively. The phase velocity ($v_f = \frac{\omega}{\beta}$) for both RH and LH TL is obtained from the dispersion equations (6.4) and (6.6). It is positive for RH-TL and negative for LH-TL. The group velocity $\left(v_g = \frac{1}{\left(d\beta/d\omega\right)}\right)$ is positive for both RH-TL and LH-TL. Therefore, the energy transport is from generator to load in both the cases, but for LH-TL case, due to the fact that the phase velocity is negative, the wave is propagated backwards (from load to generator).

6.2.2 CRLH Transmission Lines

The equivalent circuit of CRLH-TL is a combination of the equivalent circuits of RH-TL and LH-TL as shown in figure 6.2. For this circuit shown in figure 6.2 (Lai *et al.*, 2004), impedance and admittance are given by

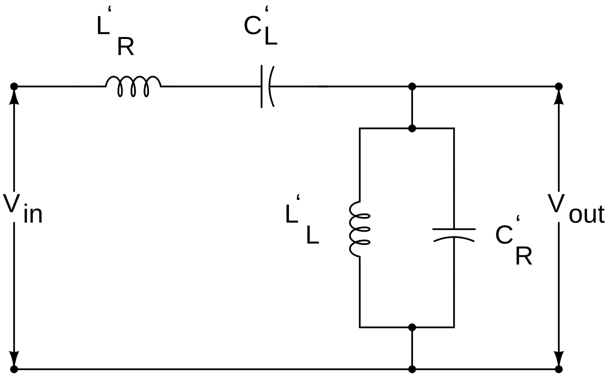


Figure 6.2: Equivalent circuit model of CRLH TL

$$Z^{'}(\omega) = j\left(\omega L_R^{'} - \frac{1}{\omega C_L^{'}}\right) \quad and \quad Y^{'}(\omega) = j\left(\omega C_R^{'} - \frac{1}{\omega L_L^{'}}\right) \tag{6.7}$$

If we consider lossless circuit ($\alpha = 0$), we get

$$\beta_{CRLH} = -\sqrt{\left(\omega L_R^{'} - \frac{1}{\omega C_L^{'}}\right)\left(\omega C_R^{'} - \frac{1}{\omega L_L^{'}}\right)} \; < 0 \;\; for \;\; \omega \; < \; \omega_{\Gamma 1} \tag{6.8}$$

$$\beta_{CRLH} = +\sqrt{\left(\omega L_R^{'} - \frac{1}{\omega C_L^{'}}\right)\left(\omega C_R^{'} - \frac{1}{\omega L_L^{'}}\right)} \; < 0 \;\; for \;\; \omega \; > \; \omega_{\Gamma 2} \tag{6.9}$$

where

$$\omega_{\Gamma 1} = min\left[\frac{1}{\sqrt{L_R^{'} C_L^{'}}}; \frac{1}{\sqrt{L_L^{'} C_R^{'}}}\right] \tag{6.10}$$

$$\omega_{\Gamma 2} = max\left[\frac{1}{\sqrt{L_R'C_L'}};\frac{1}{\sqrt{L_L'C_R'}}\right] \tag{6.11}$$

when $\omega_{\Gamma 1} < \omega < \omega_{\Gamma 2}$, β is an imaginary number and therefore γ is a real number which means that the signal on the line is attenuated and the circuit behaves as a band-stop filter. If $\omega_{\Gamma 1} = \omega_{\Gamma 2}$, then their is no stop-band. Under the condition of $\omega_{\Gamma 1} \neq \omega_{\Gamma 2}$, CRLH is said to be in unbalanced condition, while for $\omega_{\Gamma 1} = \omega_{\Gamma 2}$, CRLH is termed as balanced.

Under the condition of $\omega_{\Gamma 1} = \omega_{\Gamma 2}$, $L_R'C_L' = L_L'C_R'$. In that case,

$$\beta = \omega\sqrt{L_R'C_R'} - \frac{1}{\omega\sqrt{L_L'C_L'}} \tag{6.12}$$

If $\beta = 0$, equation (6.12) becomes

$$\omega_0 = \frac{1}{\sqrt[4]{L_R'C_L'L_L'C_R'}} \tag{6.13}$$

where ω_0 is termed as transition frequency point. The dispersion plot of Omega (ω) versus Beta (β) is obtained using equations (6.8), (6.9). Figure 6.3 shows dispersion plot comparison of balanced CRLH structure with that of Pure Left Hand (PLH) and Pure Right Hand (PRH) materials (Caloz and Itoh, 2006).

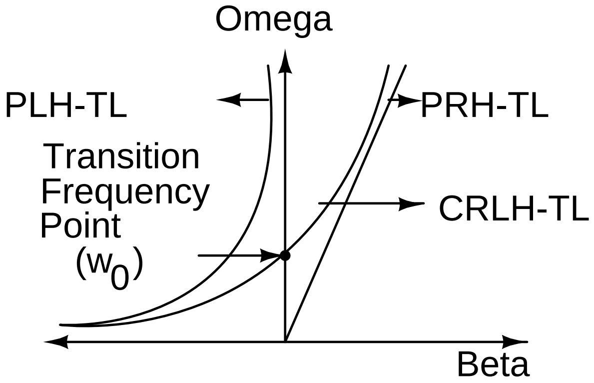


Figure 6.3: Dispersion of CRLH compared with PLH and PRH materials

In equation (6.13), ω_0 is the point at which $\beta = 0$ which implies that guided wavelength (λ_g) is ∞. The parameter λ_g is defined as c/f where c is the speed of light in free space and f is the signal frequency. This is the condition for Zero Order Resonance (ZOR). In this work, this property is used to show that the delay in the propagation of clock signals in a long interconnect can be considerably reduced by augmenting it with a CRLH structure. A ZOR behaves as a shunt LC resonator with resonance frequency of (Sanada *et al.*, 2003)

$$\omega_{ZOR} = \frac{1}{\sqrt{L_L^{'} C_R^{'}}} \tag{6.14}$$

Hence ω_{ZOR} does not depend on the physical length of the resonator. At the transition frequency ($L_R^{'} C_L^{'} = C_R^{'} L_L^{'}$), phase ($\Delta\phi_C(\omega = \omega_0)$) of the CRLH structure becomes zero.

6.3 CRLH System to Reduce the Interconnect Delay

A CRLH system to transmit a clock signal in a long interconnect line with minimum delay is shown in figure 6.4. The CRLH structure is implemented using microstrip transmission lines as shown in figure 6.5 (Zhu *et al.*, 2007). The set of microstrips in figure 6.5 form the inter digital capacitors. Both the ends of the structure are connected to the ground plane through vias forming stubs that are electrically equivalent to an inductor. The overall structure is electrically equivalent to the circuit shown in figure 6.2.

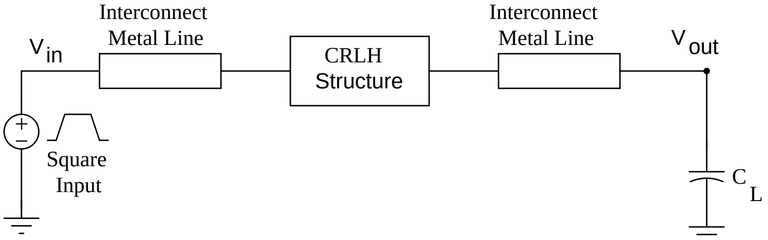


Figure 6.4: Proposed CRLH based clocking system

The contributions $C_L^{'}$ and $L_L^{'}$ in figure 6.2 are provided by the inter digital capacitors and stub inductors whereas the contributions $C_R^{'}$ and $L_R^{'}$ come from their parasitic effects and has an increasing effect with increase in frequencies. The parasitic inductance $L_R^{'}$ is due to the magnetic flux generated by the currents flowing along the digits of the

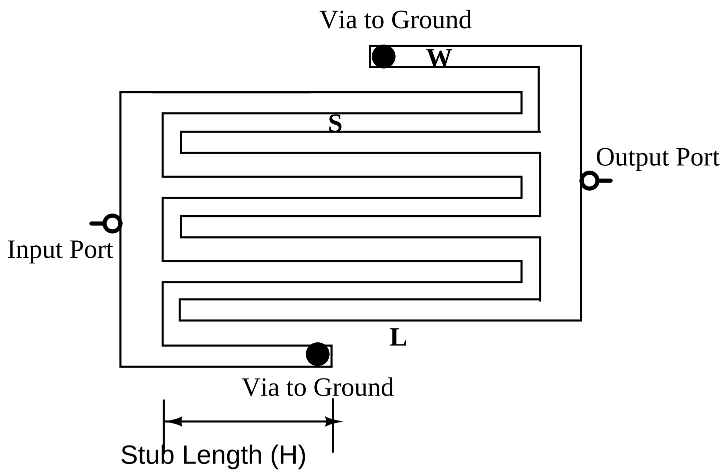


Figure 6.5: CRLH structure using microstrip lines

capacitor and the parasitic capacitance $C_R^{'}$ is due to the parallel plate voltage gradients existing between the trace and the ground plane.

6.4 Simulation Results

The structure shown in figure 6.4 is simulated using Agilent ADS. Dimensions of the structure are optimized for zero order resonance at 10 GHz. The corresponding dimensions of the CRLH structure are given in Table 6.1.

The behavior of the CRLH system is compared with that of the regular transmission line structure (termed as RH TL) using S-parameter analysis. In the simulation, receiver part is modeled as load capacitance (C_L). The transmission characteristic plot (S(2,1) in dB) of the CRLH structure is shown in figure 6.6 and is similar to that of a band pass filter response. At low frequencies, CRLH TL behaves like a PLH TL and at high frequencies, the structure behaves like a PRH TL. At all other frequencies, the transmission characteristics depend on the combination of LH and RH contributions. Whereas, characteristic plot of a TL is similar to that of a low pass filter and is shown in figure 6.7. Figure 6.8 shows the reflection response (S(1,1) in dB) at the input side of the CRLH system and the reflection is minimum at 10 GHz.

To determine the transition frequency of the CRLH system, dispersion curve (f

Table 6.1: Dimensions of the CRLH system

Structure	Dimensions	Unit
Finger length (L)	250	μm
Metal interconnect length	250	μm
Finger width (W)	8	μm
Length of the stub (H)	190	μm
Via diameter	6.4	μm
Number of fingers	3	-
Load capacitance (C_L)	100	fF

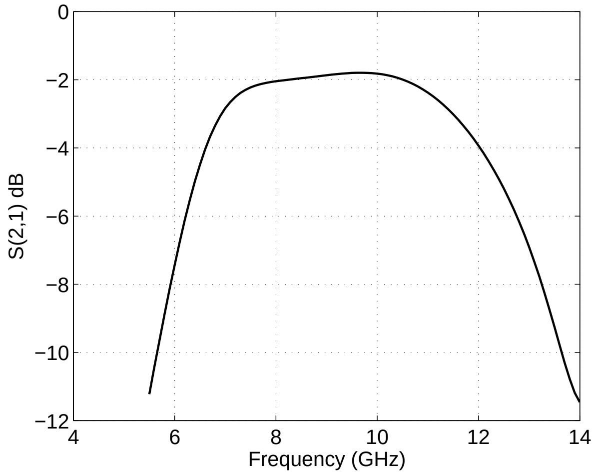


Figure 6.6: Transmission characteristic of the CRLH structure

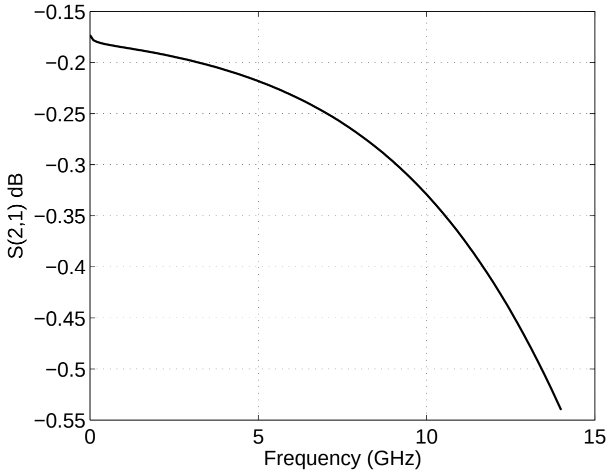


Figure 6.7: Transmission characteristics of the TL

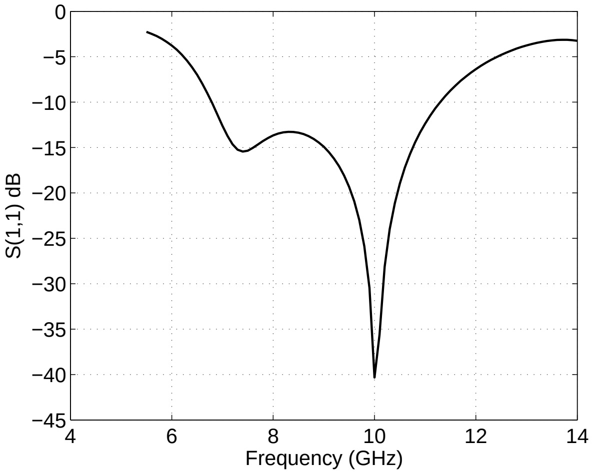


Figure 6.8: Signal reflection at the input side

versus β) is plotted as shown in figure 6.9. The propagation constant (β) is obtained from transmission parameter (S(2,1)) of the CRLH TL as

$$\beta = -\varphi^{unwrap} * S(2,1) \tag{6.15}$$

Phase of S(2,1) is a curve varying between $-\pi$ and $+\pi$ whereas the dispersion charac-

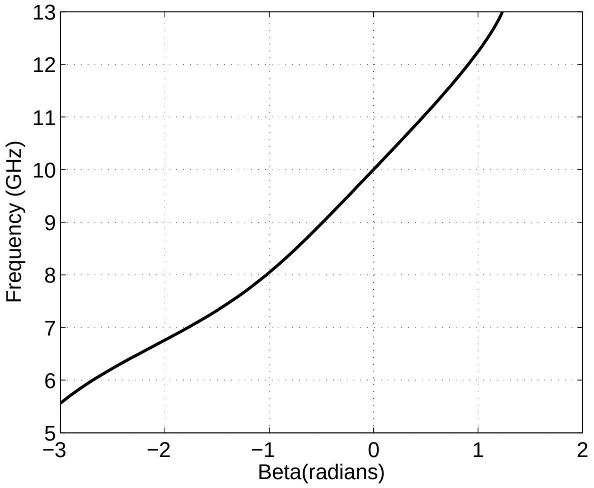


Figure 6.9: Dispersion plot of the CRLH structure

teristic β is a continuous function of frequency. Hence the phase of S(2,1) is unwrapped in order to restore the continuous nature of β. In the dispersion plot shown in figure 6.9, phase angle is zero at 10 GHz. Hence this is the zero order resonant frequency of the

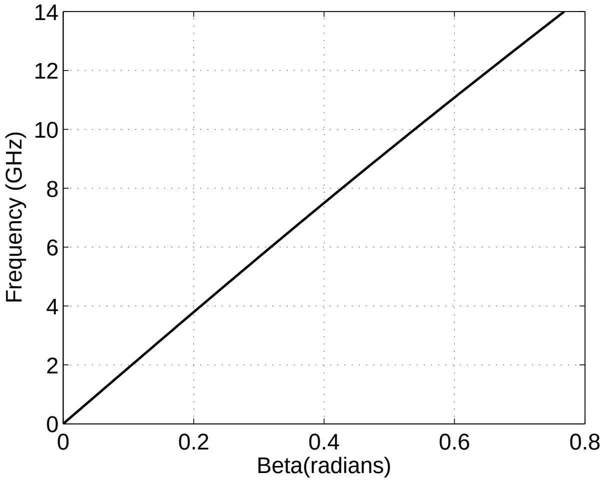


Figure 6.10: Dispersion plot of the transmission line

designed CRLH system. Whereas the dispersion plot of the transmission line is positive linear and is shown in figure 6.10.

Zero order resonant frequency depends on the shunt LC tank circuit (L_L and C_R) (equation (6.14)). The capacitance of the inter-digitized fingers is decided by its length, spacing between the digits and the width of the digits. The load capacitance (C_L) and the physical dimensions of the CRLH structure, namely, length of the stub (H), spacing between the fingers (S) and the width of the digital fingers (W) are varied to analyze their effect on the resonant frequency of the system.

Electro-magnetic simulations are performed for different geometries as shown in Table 6.2. Simulations are carried out by varying one of the parameters (H, S, W or C_L) of the CRLH structure keeping all other parameters fixed. Simulation results for different geometries shown in Table 6.2 are plotted in figures 6.11 to 6.14.

Table 6.2: Physical dimensions of the CRLH structure for different cases

	Physical Parameters	Values				
Simulation 1	H (μm)	150	170	190	210	230
Simulation 2	S (nm)	24	30	40	50	60
Simulation 3	W (μm)	8	12	16	20	23
Simulation 4	C_L (fF)	100	300	500	700	900

As the stub length increases, resonant frequency marginally decreases as shown in figure 6.11. This is due to the increase in the LH inductance value ($L_L^{'}$). When the structure is operated at the resonant frequency and as the spacing between the fingers is increased, the minimum signal reflection point shifts towards left. This is because, as the spacing between the fingers increases, $C_L^{'}$ decreases and at the same time $C_R^{'}$ increases due to increase in the voltage gradient existing between the trace and the ground plane. Hence the effective capacitance increases and the amount of reflection changes as shown in figure 6.12. Increasing the width of the fingers increases resonant frequency. As the width increases, capacitance associated with each finger increases and the total capacitance decreases because of the series connection of capacitances. On the contrary, with the increase in load capacitance, resonant frequency decreases as shown in figure 6.14.

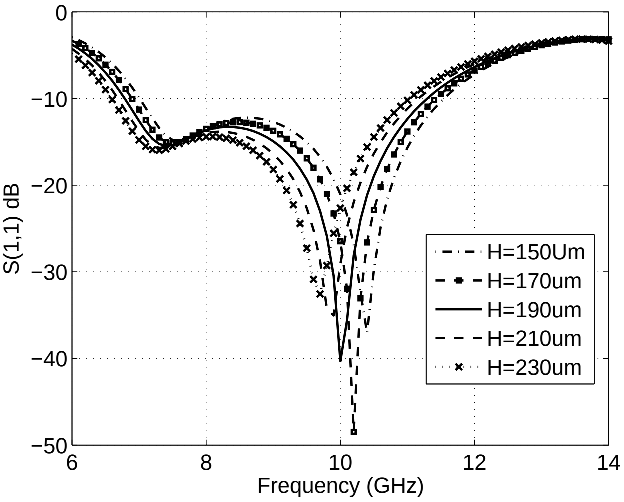


Figure 6.11: Variation in signal reflection with changes in stub length of the CRLH

The circuit shown in figure 6.4 is excited with a square wave signal (clock signal) (period 100 ps with a rise and fall time of 10 ps), the output is in phase with the input signal. Table 6.3 gives the delay comparison in a transmission line with and without the CRLH structure for different load capacitance values. From table 6.3, it is observed that the clock signal delay is considerably reduced when propagated through the transmission line with a CRLH structure. Further, delay is found to be largely independent of the length of transmission line and load capacitance.

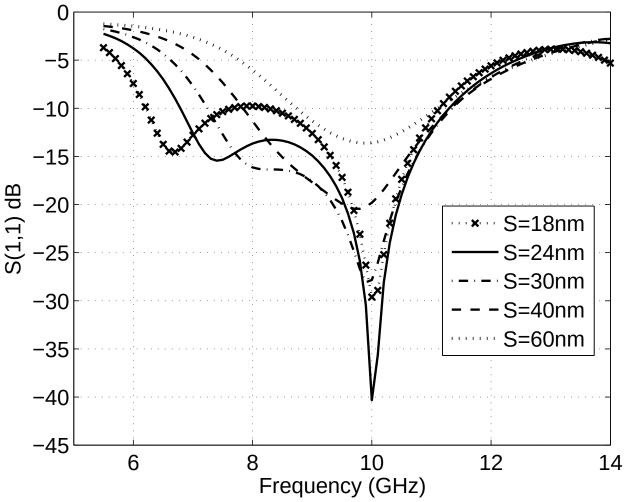


Figure 6.12: Variation in signal reflection with changes in spacing between the fingers in CRLH

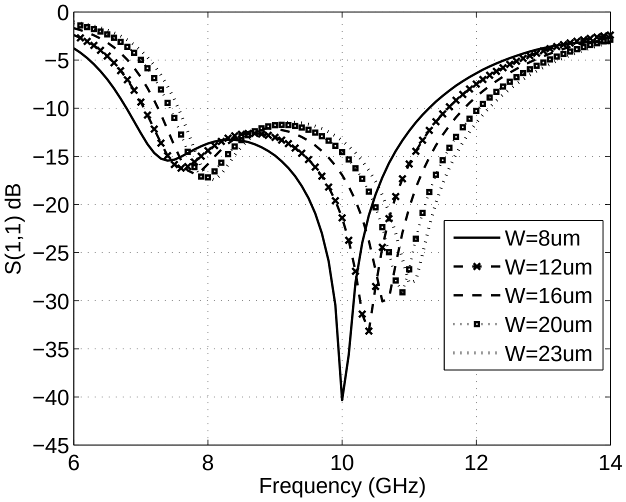


Figure 6.13: Variation in signal reflection with changes in the width of the fingers

Table 6.3: Delay comparison in a transmission line with and without the CRLH structure

Serial No.	Load Capacitance (C_L) (fF)	Delay in TL with CRLH structure (ps)	Delay in TL without CRLH structure (ps)
1	10	1	10
2	50	1	12
3	100	1	15
4	200	1	20
5	250	1	24

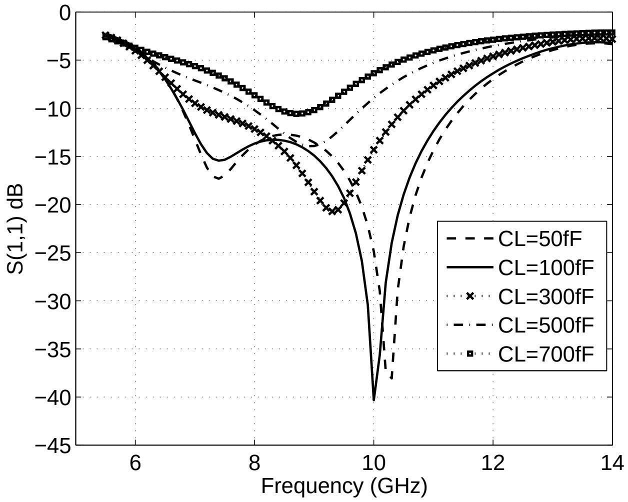


Figure 6.14: Variation in signal reflection with changes in the load capacitance

6.4.1 Example : Application of a CRLH Structure in Pipeline Stages

The overall size of the CRLH cell is in hundreds of microns even for a resonant frequency of 10 GHz. If the source node (e.g., buffer output) and the load node (e.g., input of a flip flop) of a clock network have distances less than a few tens of microns, CRLH structure will not be a good choice. In such short range clock distribution networks, metal interconnects without CRLH structures are preferred. The CRLH based clocking network is useful when clock signals need to be sent over distances exceeding 500 μm.

For system having a regularly spaced clock load such as pipeline stages, clock skew can result in data hazards. To model the efficiency of the CRLH structure for such applications, a regularly spaced series and parallel distributed load as shown in figures 6.15 and 6.16 is considered. Simulations are carried out to see the effect of variations in load capacitance (C_L) and the interconnect length (T_L) for the two models (Figures 6.15

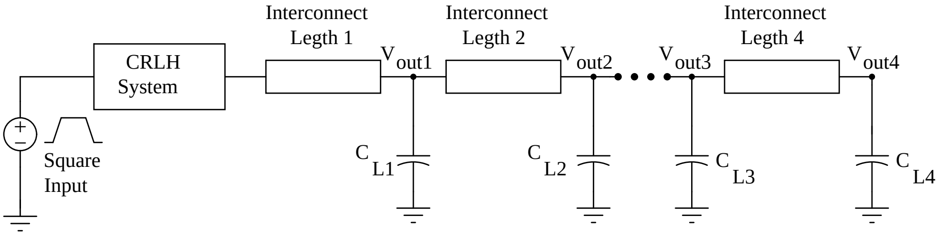


Figure 6.15: Model 1 : pipeline stages in series

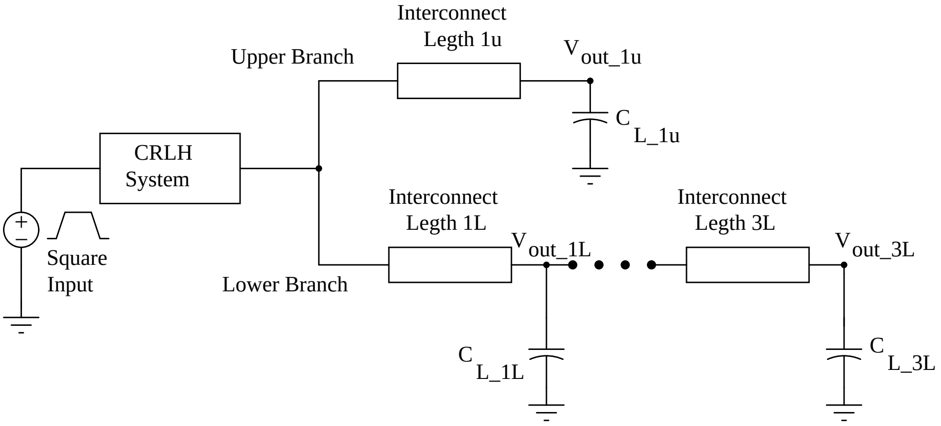


Figure 6.16: Model 2 : pipeline stages in series and parallel

and 6.16). Results in both the cases are almost identical and it is observed that the clock signal is not affected as long as the interconnect length and the load capacitance values are within certain bounds. Table 6.4 and 6.5 shows the upper bounds for the length and the load capacitance values for different number of sections of metal interconnect and load. If the length of the interconnect is increased beyond the upper bound, the amplitude of the clock signal increases. This can be attributed to the increase in the line inductance resulting in excessive overshoots and undershoots. On the other hand, if the load capacitance is increased beyond the upper limit, the clock signal attenuates due to loading effect.

Table 6.4: Upper bound on T_L and C_L for different number of sections in Model 1

Number of Sections	Maximum T_L (μm) when C_L= 50 fF	Maximum C_L (fF) when T_L= 125 μm
1	600	165
2	220	95
3	120	65
4	100	55

Table 6.5: Upper bound on T_L and C_L for different number of sections in the lower branch in Model 2

Number of Sections	Maximum T_L (μm) when C_L= 50 fF	Maximum C_L (fF) when T_L= 125 μm
1	600	80
2	200	55
3	100	38

6.5 Conclusions

In this work, it is shown that the delay in the transmission of clock signals over long interconnects can be reduced by augmenting a CRLH metamaterial structure with the interconnect line. Further, such an arrangement also eliminates the need for clock buffers at regular intervals. The designed CRLH structure is found to resonate at a frequency of 10 GHz and offer zero delay to the clock signals when operated at its resonant frequency. Analysis shows that the resonant frequency changes with the variation in the physical parameters of the structure. Further, the effect of variations in the load capacitance and the interconnect length on resonant frequency and signal delay are studied. It is found that the delay in clock signal is not affected as long as the interconnect length and the load capacitance values are within certain bounds.

CHAPTER 7

Conclusions and Scope for Future Work

7.1 Thesis Outcome

This thesis mainly focuses on improving the performance of on-chip intermediate/global interconnect lines in GHz regime. The issues addressed in this thesis include modeling, crosstalk estimation in multi-coupled interconnects, minimizing the signal reflection at the interconnect-via junction, reducing delay in long interconnect lines by using resonant interconnect structures and reducing the clock delay and skew by using CRLH metamaterial in the clocking network.

In this thesis, interconnects are modeled as distributed RLGC network using state space approach. Generalized state space matrices are derived for single, coupled, **L** and **T** type interconnects. Models of coupled, **L** and **T** type interconnects include mutual inductance and coupling capacitance effects between the adjacent lines and the branched segments. Since the derived state space matrices are modular in nature, interconnect metrics for any length and for any arbitrary Manhattan geometry can be estimated. This is demonstrated by modeling a generic interconnect of tuning fork structure and the results are verified by comparing the model output with SPICE simulation.

Crosstalk noise estimation in the victim line of the two-coupled interconnects is presented using the generalized state space matrices. Also, it is demonstrated that these models can be extended to estimate the coupled noise voltages in the victim lines of multi-coupled interconnects for different input switching conditions. Further, it is shown that the order of a large RLGC network can be effectively reduced to a lower order by Model Order Reduction technique using Moment Matching method to reduce the computational complexity of estimating the interconnect metrics.

A resonant interconnect network employing an active inductor for signal delay reduction is presented. When the data is sent at the resonant frequency of the network, the delay introduced by the interconnect is found to be minimum. Since clock signals switch continuously, this scheme can be effectively used for clock signals as well. It is shown that by replacing passive inductor with an active inductor in the resonant interconnect section, the latency is reduced by 24%. From the calculations, it is found that the silicon area required to fabricate an active inductor of 7.5 nH is approximately 24 times less than that of a passive inductor. In addition to this, analysis of crosstalk noise voltage(s) on the victim line(s) of the coupled-interconnects employing active inductors is found to be considerabely reduced.

At GHz frequencies, interconnects behave as transmission lines and the impedance discontinuity at interconnect-via junction causes signal reflections. A methodology to minimize the signal reflection at the interconnect-via junction by incorporating an additional capacitance for impedance matching is presented. In the two-layer interconnect model connected through a via, signal reflections are reduced to less than -10 dB in the frequency range of 1 to 10 GHz and below -35 dB at the tuned frequency of 5 GHz. The proposed method is applied to a six-layer interconnect structure and the signal reflection is found to reduce considerably. The above method can be extended to different operating frequencies by incorporating digitally tunable capacitive loading.

To reduce the latency/skew of clock signals when transmitted over long networks, CRLH metamaterial structure as part of the clock network to eliminate the clock latency is presented. Also, such an arrangement eliminates the need for clock buffers at regular intervals. The CRLH structure can be designed to resonate at any frequency (at 10 GHz in this work) and is found to offer almost zero delay over long clock networks.

7.2 Scope for Future Work

The present work deals with improving the performance of Cu/Low-K interconnects by making use of circuit level and structural modifications. The various modifications suggested in the thesis for improving the interconnect performance is based purely on simulation results. However, the actual improvements can be seen only when these are implemented at a given technology node and compared with the simulation results. The actual implementation can be taken-up as a future work.

At an architectural level, 3-D IC's are gaining prominence for variety of reasons and reduction of interconnect delay is one key parameter. 3-D IC's can also facilitate integration of heterogeneous technologies in one single chip. However, all these advancements will take considerable time before they become industry standards.

Some of the recent works have shown the comparison of Carbon Nano Tubes (CNT) with copper interconnects and suggest CNT's as future interconnects. However, the use of CNT's as interconnects in highly complex IC's is yet to be demonstrated. Thus a performance comparison of the schemes suggested in this work with CNT's would give a better understanding of how the technology could evolve in future.

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LIST OF PAPERS BASED ON THESIS

Journal Publications

1. Soorya Krishna K, Pramod M and M.S. Bhat. Modeling of Single, Coupled, L and T type Interconnects using State Space Approach. *International Journal of Signal and Imaging Systems Engineering, Inderscience Publications*, 2(4), 216–223, October 2009 (DOI : 10.1504/09.33785).

2. Soorya Krishna K and M.S. Bhat. Minimization of Via Induced Signal Reflection in On-Chip High Speed Interconnect Lines. *Circuits, Systems and Signal Processing, Springer Publications*, 31(2), 689–702, April 2012 (DOI : 10.1007/s00034-011-9339-0).

3. Soorya Krishna K and M.S. Bhat. Impedance Matching in Multi-Layer Interconnect Structures to Minimize Signal Reflections in High Speed Applications. *International Journal of Computer and Electrical Engineering*, 4(3), 345–349, June 2012 (ISSN: 1793-8163).

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