WIDELY TUNABLE BANDWIDTH ULTRA LOW POWER CONTINUOUS TIME FILTERS FOR BIOMEDICAL APPLICATIONS

Thesis

Submitted in partial fulfillment of the requirements for the degree of
DOCTOR OF PHILOSOPHY

by

JAYARAM REDDY M K

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING,
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA,
SURATHKAL, MANGALORE -575025

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DECLARATION

I hereby ***declare*** that the Research Thesis entitled **WIDELY TUNABLE BANDWIDTH ULTRA LOW POWER CONTINUOUS TIME FILTERS FOR BIOMEDICAL APPLICATIONS** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** in **Department of Electronics and Communication Engineering** is a ***bonafide report of the research work carried out by me***. The material contained in this research thesis has not been submitted to any University or Institution for the award of any degree.

Jayaram Reddy M.K.

Jayaram Reddy M K,
Reg. No.: 145030/EC14F04
Department of Electronics and
Communication Engineering.

Place: NITK-Surathkal.
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CERTIFICATE

This is to certify that the Research Thesis entitled **WIDELY TUNABLE BAND-WIDTH ULTRA LOW POWER CONTINUOUS TIME FILTERS FOR BIOMEDICAL APPLICATIONS** submitted by **JAYARAM REDDY M K** (Register Number: 145030EC14FO4) as the record of the research work carried out by him, is accepted as the *Research Thesis submission* in partial fulfillment of the requirements for the award of degree of **Doctor of Philosophy**.

19/10/2020

Prof. Laxminidhi T.
Research Guide and
Chairman-DRPC
Dept. of E & C Engg.
NITK Surathkal - 575025

(Signature with Date and Seal)

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My Dear Parents

Abstract

This research intends to focus on filter architectures for bio-medical applications. The proposed filter architectures are designed to operate on a supply voltage of 1.8 V in 0.18 μm standard CMOS process from UMC technologies.

Initially, this thesis proposes a novel architecture for realizing very low transconductance values with tunability. This transconductor architecture makes it possible to realize a fully differential filter without the need of explicit common-mode feed back (CMFB) circuit. Using the proposed transconductor a fourth-order, low pass Butterworth g_m-C filter with tunable bandwidth has been designed for biomedical signal processing front-ends. This novel filter architecure has two bandwidth tuning schemes, a resistor based tuning (R-tuning) and a switched transconductor based tuning (D-tuning). With these tuning techniques, the filter is made tunable in the range 30 mHz-100 Hz. The filter operating on 1.8 V supply is found to offer a DR of 56 dB consuming a power of 1.14 μW. In terms of Figure-of-Merit (FoM), the proposed filter is found to be on par with the filters reported in literature.

This thesis also proposes a second-order low pass Butterworth filter with tunable bandwidth capable of offering a dynamic range of 91.86 dB. The proposed filter is based on a sub-threshold source follower. The main idea is to exploit the strengths of sub-threshold source follower circuit, like low noise, low output impedance, high linearity and low power. The transistor bias currents are switched to enable the bandwidth tuning in the range 4 Hz - 100 Hz. A PTAT current reference circuit helps to keep the bandwidth intact across process, voltage and temperature variations. In terms of noise and dynamic range the reported filter is better than previous works found from the literature. The filter consumes 25.9 nW making it a potential candidate for portable biomedical applications.

Finally, this thesis proposes a scheme to enhance the output resistance of a differential amplifier. A negative resistance is used to cancel the output resistance of the differential amplifier. This inturn is achieved through a transimpedance based loop. It is proved that the proposed scheme can

give a gain enhancement of about two folds (in dB) compared to the gain of basic differential transconductor, without loss in linearity. An OTA designed using this scheme is found to offer least sensitivity of gain boost over output voltage swing across process corners, at nominal voltage and temperature, when compared to other methods found in literature. A first order filter is designed using the proposed r_o enhanced OTA. The filter offer cut-off frequency down to 0.5 Hz without any switching scheme, and more significantly without the loss of DC gain.

Keywords: Analog filter; Low cut-off frequency; Bio-medical; Source follower; High dynamic range; Conductance cancellation; Gain enhancement; High gain OTA;

Contents

List of Figures

List of Tables

Abbreviations

g_m-C	Transconductor-Capacitor
OTA	Operational transconductance amplifier
THD	Total harmonic distortion
HD_3	Third harmonic distortion
LPF	Low pass filter
MOSFET	Metal oxide semiconductor field effect transistor
NMOS	N-channel metal oxide semiconductor
PMOS	P-channel metal oxide semiconductor
CMOS	Complementary metal oxide semiconductor
RLC	Resistor-Inductor-Capacitor
RC	Resistor-Capacitor
ECG	Electrocardiogram
EMG	Electromyogram
EEG	Electroencephalogram
LFP	Local field potentials
SoC	System-on-chip
ESD	Electrostatic discharge
CD	Current division
SD	Source degeneration
BC	Body control
MIFG	Multiple input floating gate
SNR	Signal to noise ratio
FoM	Figure-of-merit
SC	Switched Capacitor
DR	Dynamic range
DC	Direct current
CMFB	Common mode feedback
UMC	United Microelectronics Corporation
PVT	Process, supply voltage and temperature
IRN	Input referred noise
D	Duty ratio
PTAT	Proportional to absolute temperature
SSF	Sub-threshold source follower
OSR	Output swing range
PM	Phase margin

.

Notations

f	Frequency in Hz
ω_p	Pole frequency in radians per sec
f_c	Cut-off frequency in Hz
g_m	Gate transconductance in Siemens
g_{mb}	Bulk-transconductance in Siemens
Q	Quality factor
L	Channel length of the MOSFET
W	Channel width of the MOSFET
V_{GS}	Gate-source voltage of the MOSFET
V_{DS}	Drain-source voltage of the MOSFET
V_{BS}	Bulk-source voltage of the MOSFET
k	Boltzmann Constant
T	Absolute temperature
q	Electronic charge
μ	Carrier mobility
C_{ox}	Gate-oxide capacitance
V_{TH}	Threshold voltage
V_T	Thermal voltage
1/f	Flicker noise
η	Sub-threshold slope factor
γ	Noise co-efficient
K_F	Flicker noise coefficient
γ_o	Body effect coefficient
φ_{FB}	Bulk Fermi potential
N	Filter order

.

Chapter 1

INTRODUCTION

Naturally occurring signals are typically weak analog signals, usually corrupted by noise. They must be amplified and filtered to improve the signal-to-noise ratio before converting them to digital for further processing. Amplifiers and filters along with Analog-to-Digital Converters form the analog front end of a typical signal processing system. Filters in analog front end help to eliminate out of band noise and also used as anti-alias filters. The frequency of the analog signals generated at frontiers such as seismology, biology, astrophysics, geophysics typically fall in the range of few tens of milli-hertz to few hundred hertz.

Bio-electric signals are signals generated by the cells and tissues of the biological system. These signals are predominantly used to extract information related to the health state of any biological system. Recording and evaluation of these bio-electric signals helps in diagnosing and monitoring the patients health and also in timely treatment of diseases. Bio-electric signals such as electrocardiogram (ECG), electromyogram (EMG), electroencephalogram (EEG), and Local field potentials (LFP) are small signals of low frequency usually found in the 10 mHz to 10 KHz frequency range (Webster 2009). Figure 1.1 Harrison (2007) shows a typical range of signal amplitude and frequency contents of such bio-signals.

Historically, standard medical instruments used for measurements have been bulky and involves attaching of electrodes or sensors to the patient to be monitored. This procedure is acceptable for the short term monitoring, however for long-term monitoring it is not comfortable. The cost of these conservative procedures are significantly high due to the long pre-testing and many medical regulations. However, by using the recent innovations in bio-medical instruments like wearable and implantable de-

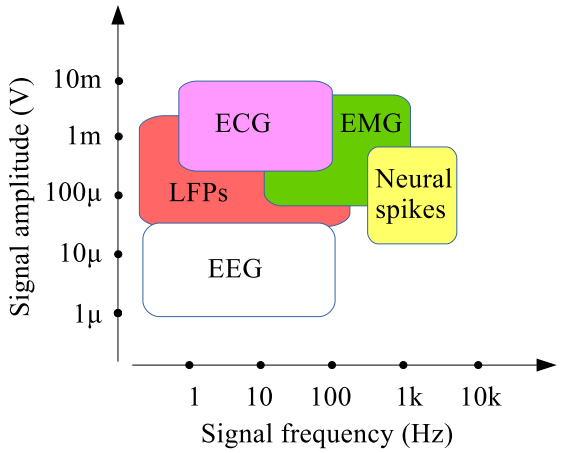


Figure 1.1: Frequency content and amplitude distribution of common bio-potentials

vices the same functionality can be implemented with low cost, high performance and smaller form factor.

Block diagram of a typical bio-potential signal acquisition system is shown in Figure 1.2 (Zhang *et al.* 2013). After converting a physiological signal into an electrical signal by the transducer, an analog pre-processing block is required to amplify and filter the signal before sending it for further processing. Amplification and filtering helps to enhance the quality of the desired bio-potentials by reducing the unwanted noise. The filters are therefore inevitable in analog integrated circuits designed for processing such signals.

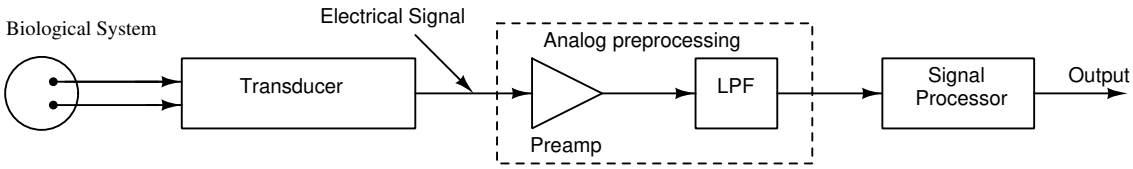


Figure 1.2: Block diagram of bio-potential signal acquisition system

This research focuses on the design of filters for such bio-medical acquisition systems requiring low cut-off frequencies with low power consumption and smaller silicon area.

1.1 Motivation

There are a number of filter topologies found in the literature. A few important and common filter topologies are,

- Passive RLC filters
- Active-RC filters
- MOSFET-C filters
- Switched capacitor filters and
- Transconductor-capacitor $(g_m - C)$ filters

Passive RLC filters are simple in architecture and consume very low power. Figure 1.3 shows the schematic of a first order low-pass filter realized using the passive RC topology.

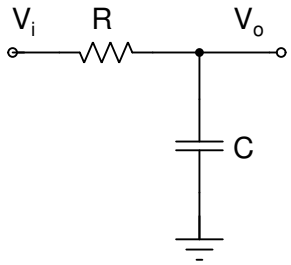


Figure 1.3: Passive-RC filter

The transfer function for passive filter is of the form,

$$H(s) = \frac{1}{1 + sRC} \tag{1.1}$$

However, for realizing higher order filters, cascading of filters cannot be adopted directly without accounting for the loading from the following stage. Another limitation is that for realizing filters having high quality factor (Q), inductors have to be used along with resistors and capacitors. Realizing inductors in integrated circuits, especially for low frequency filters where the desired inductor will be large (of the order of milli henries), is impractical as it would occupy a significantly large silicon area.

An alternative approach is to use active filter, where inductors are realized using a combination of capacitors, resistors and active elements. The use of active elements

also allows easy cascading of sections. For these reasons active filters are widely used in integrated circuits.

Figure 1.4 shows a first order Active-RC low-pass filter. The filter transfer function has the same form as in (1.1) except that it has a negative sign.

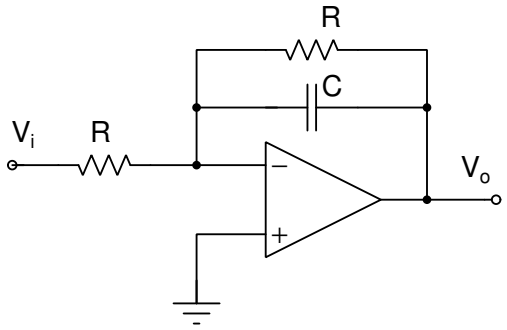


Figure 1.4: Active-RC filter

Passive and Active-RC filters are not preferred for realizing low bandwidth filters. This is because, the cutoff frequency of these filters is of the form given in (1.3),

$$f_0 = \frac{1}{2\pi\,(RC)} \tag{1.2}$$

For realizing a filter with 100 Hz bandwidth, if an on-chip capacitor of 1 pF is chosen, the value of R required would be as large as 1.59 $G\Omega$. The value of R further scales up, as the bandwidth requirement of the low-pass filter goes down. Realizing such a large value of passive resistors on-chip is quite impossible.

In MOSFET-C filters, MOSFET operating in linear region is used to implement tunable linear resistances (Neshatvar *et al.* 2014, Harrison and Charles 2003). This technique is quite popular because of its simplicity and ease in tunability achieved by simply changing the gate voltage of MOS resistor. A basic MOSFET-C integrator circuit is shown in the Figure 1.5. The time constant achieved in such filters is decided by $R_{ch}C$ product, where R_{ch} is the channel resistance of the transistor M_1. The channel resistance is limited to few tens of mega ohms which is not sufficient to implement filters with very low cut-off frequencies. Also, the linearity of the circuit depends on the linearity of the MOS resistance. To achieve good linearity the transistors are often driven by a large gate voltage. This typically necessitates voltage boosting circuits for realizing gate voltage above the available supply voltage.

Switched-capacitor filters are popular in biomedical systems. A schematic of

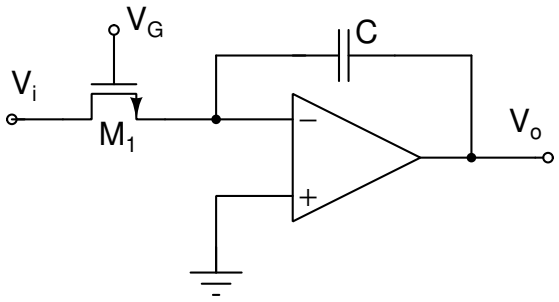


Figure 1.5: MOSFET-C integrator

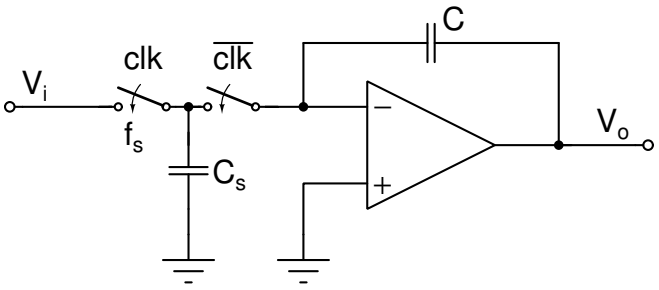


Figure 1.6: Switched capacitor integrator

switched capacitor integrator used in such filters is shown in figure 1.6. Here the resistance is replaced by a switched capacitor circuit such that $R = 1/(f_s C_s)$ where f_s is the frequency at which the switches are operated and C_s is the switching capacitance (Sarpeshkar 2010).

The cutoff frequency of such filters takes the form as in (1.3)

$$f_0 = \frac{f_s C_s}{2\pi C} \tag{1.3}$$

However, for large time constants (low bandwidth), switched capacitor (SC) topologies require large capacitor ratios (C/C_s). This demands a large power for the opamp as it has to drive high capacitance of C. Also, stability of the loop can be an issue with the common Miller compensation since it tries to make first stage output node of the opamp a dominant pole contributor. In addition, switched capacitor filters suffer from leakage problem in advanced nano-meter processes, in which case leakage reducing mechanism is necessary to retain the signal. For the above reasons, SC filters are found only upto a bandwidth of few hundreds of hertz on the lower side.

The $g_m - C$ filters are often preferred for high frequency filters due to their open-loop architecture. However, large time-constants can also be practically achieved in this type of filters. A simple first order $g_m - C$ low-pass filter is shown in Figure 1.7. The transfer function of this filter is given in (1.4).

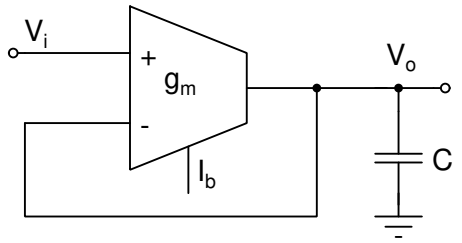


Figure 1.7: First order $g_m - C$ filter

The cutoff frequency in such realizations is,

$$H(s) = \frac{1}{1 + s\left(\frac{C}{g_m}\right)} \tag{1.4}$$

The cutoff frequency of the filter is decided by the ratio $\frac{g_m}{C}$. Thus, lower cutoff frequencies can be practically achieved by increasing C and/or decreasing g_m. If we consider increasing the capacitance alone, the value of capacitance required becomes large. Off-chip capacitance values as high as few micro-farads can be used. However, off-chip capacitors increase the pin-count of the IC as such filters are not stand-alone systems rather a part of the system in total, especially in system-on-chip (SoC) applications. In addition, since the transconductors are typically of very low value, they suffer from the possible leakages at the bond pads and electro-static-discharge (ESD) protection circuits when used with off-chip capacitors.

For SoC applications the filters have to be realized on-chip, calling for the use of on-chip capacitances. In such a case the capacitances are limited to a few tens of pico-farads due to the limitations posed by silicon area and associated cost.

With the limited value of capacitance available on-chip, creating a large time constant for very low frequencies is a challenging task. For very low values of g_m, of the order of sub-micro siemens, MOSFETs have to be generally operated in weak-inversion region. However, linearity has to be traded-off. Therefore, realizing extremely low g_m preserving linearity over the input range and hence the acceptable dynamic range is a real challenge.

One more advantage of $g_m - C$ filters is that their bandwidth can be easily programmed by tuning g_m which in turn can be easily attained by varying the bias current I_b. Hence they occur as a natural choice for low frequency applications, less than 100 Hz. Accordingly many filters in the literature are found to use $g_m - C$ toplology for low frequency applications.

1.1.1 Low Power IC Design Challenges

Power consumption is one of the major concerns in the design of circuits targeted for portable biomedical applications like wearable and implantable devices. The system being powered from battery, the designs are expected to consume as low power as possible, down to the order of micro-to-nano watts. In CMOS technology, it is common to operate MOS transistors in the sub-threshold or weak inversion region by applying very low bias currents in the order of a few μA's down to a few nA's Solís-Bustos *et al.* (2000) Surachoke and Sawigun (2018)Lee *et al.* (2018) thus resulting power of the order of micro/nano watts.

However, operating MOS transistors in weak inversion region with low bias currents leads to the following issues:

- In weak inversion region, as the current equation is governed by exponential function, the I-V characteristic of the MOS transistor is highly non-linear(Enz *et al.* 1995).
- The effect of transistor mismatches in weak inversion region are more, when compared to transistors operating in strong inversion region because of low current densities(Kinget 2005).
- As the design is for low frequency applications, flicker noise($1/f$) is one of the important parameter of concern. To suppress $1/f$ noise large sized transistors are required thus occupying large chip area(Veeravalli *et al.* 2002*a*, Sawigun and Serdijn 2016).

Designing filters, offering desired performance parameters, under the influence of above mentioned issues is quite challenging. Any effort on filter design offering a sufficient dynamic range with reduced power or in other words offering state of the art Figure-of-Merit (FoM) is worth investigating. And this thesis is the result of the efforts in this direction for realizing filters having tunable bandwidth.

1.2 Prior Work

In literature, several works have reported the design and implementation of OTAs and low frequency $g_m - C$ filters for biomedical applications. However, in this section the works reporting the techniques used to achieve low transconductance and the technique used to simulate large capacitors are discussed along.

To reduce the cut-off frequency, increasing the capacitance beyond few tens of picofarads is limited by silicon area and cost. Higher value of capacitances have been found to be emulated through Impedance scaling techniques in (Silva-Martinez and Salcedo-Suñer 1997, Silva-Martinez and Vazquez-Gonzalez 1998). The impedance scaling increases the effective capacitance on chip. The principle of impedance scaling is as shown in Figure 1.8. If the g_m of the diode connected transistor is large enough,

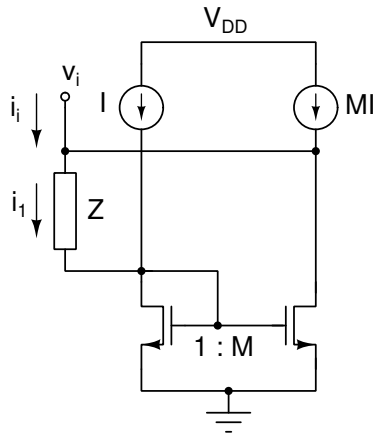


Figure 1.8: Impedance scaling technique

than the small signal input current i_i can be approximated to (1.5)

$$i_i = \frac{M+1}{Z}\, v_i \tag{1.5}$$

From (1.5), the equivalent input impedance becomes,

$$Z_i = \frac{v_i}{i_i} = \frac{Z}{M+1} \tag{1.6}$$

If Z is realized as a capacitance C, than the effective capacitance seen at the input

terminal is C scaled up by a factor $(M+1)$ i.e.

$$C_i = (M+1)C \tag{1.7}$$

In fact, the admittance seen at v_i has a pole at $-\frac{g_m}{C}$ and this pole has to be placed sufficiently far away from the desired filter bandwidth. This demands g_m to be sufficiently large. In addition, the M is the scaling factor and larger the M more will be the current requirement. Therefore, the circuit altogether results in increased noise and power consumption. This capacitance scaling technique has been used to realize capacitance of the order of 200 pF using 5 pF in Solís-Bustos *et al.* (2000). Also, an attempt has been made to improve the circuit. However, noise and power have still been a concern.

As has been mentioned already, the low cutoff frequencies can be achieved through transconductance (g_m) reduction techniques too. Commonly, the basic transconductor unit is modified to reduce the effective g_m. The various g_m reduction techniques available in literature as reported in Veeravalli *et al.* (2002*b*), Solís-Bustos *et al.* (2000) and their limitations are discussed below.

In current division technique (Silva-Martinez and Salcedo-Suñer (1997)), current mirrors or splitters with large division ratios are used to reduce the output current of the transconductor and hence the effective transconductance. The basic idea of the current division technique is as shown in Figure 1.9

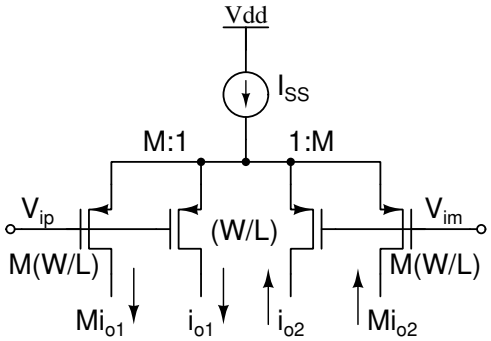


Figure 1.9: Current division technique.

The effective transconductance achieved from the current division is given by

$$g_{m,eff} = \frac{g_m}{(1+M)} \tag{1.8}$$

where M is the ratio of transistors used for the current division. The current division technique is also used in Solís-Bustos *et al.* (2000), Arnaud *et al.* (2006) to achieve large time constants. The limitations are large circuit area, limited dynamic range and low current ratio accuracy as reported in Silva-Martinez and Salcedo-Suñer (1997) and Zhou and Chakrabartty (2015). In addition, use of large division ratios increases the offset voltage.

Use of Multiple Input Floating Gate (MIFG) based transconductor is another technique found in literature to get low g_m (El Mourabit *et al.* 2005,Veeravalli *et al.* 2002*a*). The schematic of such a transconductor is shown in Figure 1.10. Here, floating gate

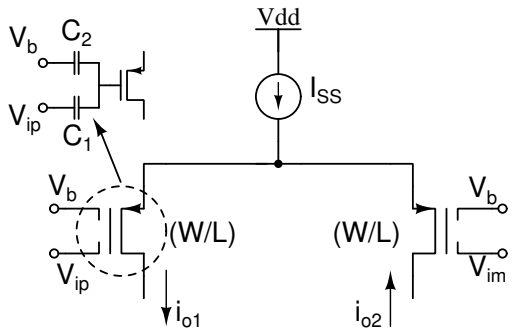


Figure 1.10: Multiple input floating gate technique

MOS transistors with two inputs (the bias voltage V_b and input $V_{ip,m}$) are used as the input transistors. These transistors capacitively attenuate the voltage at the input, thus reducing the effective g_m. The effective g_m is given by

$$g_{m,eff} = \left(\frac{C_1}{C_1 + C_2}\right) g_m \tag{1.9}$$

where C_1 and C_2 are the poly capacitors coupled to the input. For proper operation the value of capacitors C_1 and C_2 must be greater than parasitics. The drawbacks are large circuit area due to large capacitor ratios required, limited tunability and increased input referred noise.

Source degeneration technique is also used to reduce the g_m in Veeravalli *et al.* (2002*b*). Figure 1.11 shows the transconductor adopting source degeneration technique. The effective g_m obtained is given by

$$g_{m,eff} = \frac{g_m}{1 + g_m R} \tag{1.10}$$

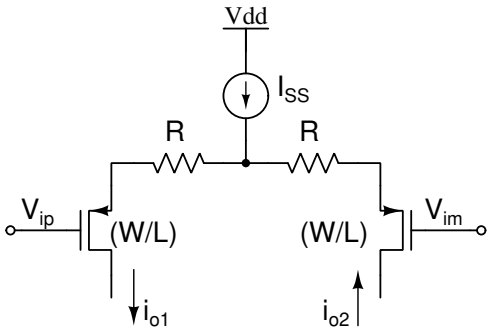


Figure 1.11: Source degeneration technique

The drawback of the technique is large value of R required to achieve low g_m results in more circuit area and noise.

Bulk driven transconductor topology shown in figure 1.12 is also found as a method to realize low bandwidth filters (Cotrim and de Carvalho Ferreira 2012 ,Veeravalli *et al.* 2002*b*). Here, the input is applied to the bulk terminal rather than gate terminal. This is to take advantage of lower bulk transconductance (g_{mb}) typically around 0.2 to 0.4 times gate transconductance (g_m) as per (1.11) .

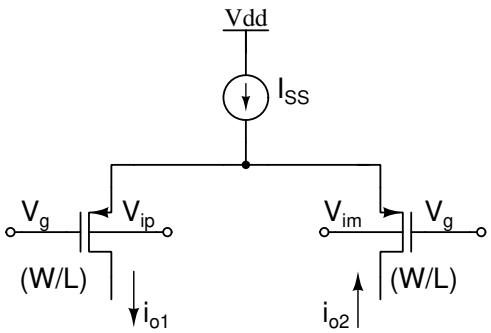


Figure 1.12: Bulk driven technique

$$g_{mb} = \left(\frac{\gamma_o}{2\sqrt{2\varphi_{FB} + |V_{BS}|}} \right) g_m \tag{1.11}$$

In (1.11), γ_o is the body effect coefficient, φ_{FB} is the bulk Fermi potential. The drawbacks of this technique are it is very much process dependent and also it has finite input impedance.

Filter based on the triode region transconductor is also found to be used for achieving low values of g_m (Bruschi *et al.* 2007, Bruschi *et al.* 2005). The core of the

transconductor is simple NMOS differential pair shown in Figure 1.13. For the tran-

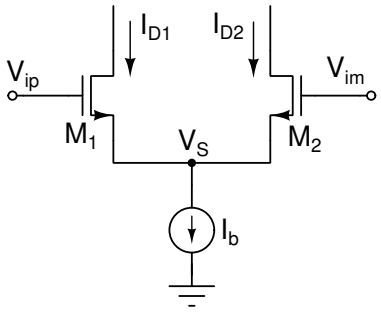


Figure 1.13: Basic source coupled differential pair

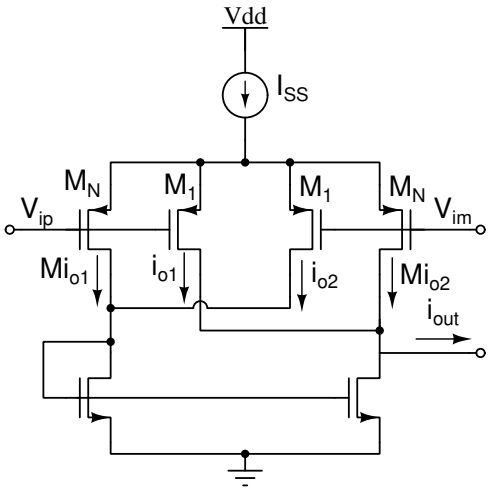


Figure 1.14: Current cancellation technique

sistors biased in triode region with same V_{DS}, the drain currents I_{D1} and I_{D2} are given by:

$$I_{D1,2} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS1,2} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{1.12}$$

from which one can write

$$I_{D1} - I_{D2} = \beta V_{DS} (V_{ip} - V_{im}) \tag{1.13}$$

The transconductance is thus given by

$$g_{m,eff} = \beta V_{DS} \tag{1.14}$$

where $\beta = \mu_n C_{ox} \frac{W}{L}$, $\frac{W}{L}$ is the aspect ratio of the input transistors, μ_n is the electron mobility and C_{ox} is the gate oxide capacitance. Here small value of transconductance is obtained by keeping V_{DS} to a small value. This is achieved through the use of an additional feedback amplifier resulting in increased circuit area, noise and complexity.

Another technique used to reduce g_m is current cancellation (Silva-Martinez and Salcedo-Suñer 1997, Solís-Bustos *et al.* 2000). The technique is shown in Figure 1.14 and the transconductance is given by

$$g_{m,eff} = \left(\frac{M-1}{M+1}\right) g_m \tag{1.15}$$

where M is the ratio of transconductance of transistors M_N to M_1. Note that here a partial positive feedback is used. From (1.15), transconductance achieved can be very small if the value of M is close to 1. However with M close to unity, the transcondutor is highly sensitive to mismatches and prone to the risk of gain inversion in presence of mismatch.

Table 1.1 summaries various g_m reduction techniques found in literature.

1.3 Thesis Contribution

Observing the limitations of existing g_m reduction techniques, it is felt there is a scope for new techniques for realizing low bandwidth $g_m - C$ filters. Also, designing power efficient architecture offering a descent dynamic range is the need of the hour. Accordingly, a novel g_m reduction technique has been proposed. The proposed technique pays the way to realize very low transconductance value with tunability. In addition, the proposed transconductor architecture makes it possible to realize a fully differential filter without the need of explicit common-mode feed back (CMFB) circuit, which otherwise is essential in classical gyrator based filter design approach to maintain the output common mode DC voltage of every stage preferably to a common reference value (same as input common mode DC) when realizing higher order filters using cascade of sections (Pramod and Laxminidhi (2010), Chatterjee *et al.* (2005)).

Using the proposed transconductor a fourth-order, low pass Butterworth g_m-C filter with tunable bandwidth has been designed in 0.18 μm CMOS process from UMC Technologies.

A Source follower has the highest linearity as the source node can swing to the level

Table 1.1: Summary of g_m reduction techniques found in literature and their limitations.

Technique	**Paper**	**Effective g_m**	**g_m (S)**	**B.W (Hz)**	**Limitations**
Current Division	Silva-Martinez and Salcedo-Suñer 1997	$\frac{g_m}{1+M}$	–	10	Circuit area
	Solís-Bustos *et al.* (2000)		–	2.4*	Current ratio accuracy
	Bruschi *et al.* (2004)		20p	0.225	Output dynamic range
	Arnaud *et al.* (2006)		69n	–	Offset voltage
Multiple Input Floating Gate	El Mourabit *et al.* (2005)	$\left(\frac{C_1}{C_1+C_2}\right) g_m$	–	200	Large capacitor ratio
	Veeravalli *et al.* (2002*a*)		5n	5*	Input referred noise
	Veeravalli *et al.* (2002*b*)		9.2n†	–	Limited tunability
Source Degeneration	Veeravalli *et al.* (2002*b*)	$\frac{g_m}{1+g_mR}$	9.3n†	–	Large area for R
	Lee and Cheng (2009)		1.63	250	Thermal noise of R
Bulk Driven	Veeravalli *et al.* (2002*b*)	$\left(\frac{\gamma_o}{2\sqrt{2\Psi_{FB}+V_{SB}}}\right) g_m$	10n	0.17$^\blacklozenge$	Finite input impedance
	Cotrim and de Carvalho Ferreira (2012)		66n	–	Process dependent
	Liu *et al.* (2012)		2.1n	40	
Triode Region	Bruschi *et al.* (2007)	$g_{m,eff} = \beta V_{DS}$	5n	15	Circuit area, noise
	Bruschi *et al.* 2005		5n	–	Circuit complexity
Current Cancellation	Silva-Martinez and Salcedo-Suñer (1997)	$g_{m,eff} = \left(\frac{M-1}{M+1}\right) g_m$	–	–	Gain inversion
	Solís-Bustos *et al.* (2000)		–	2.4*†	Sensitive to Mismatch

* With impedance scaling for load capacitor † With current division $^\blacklozenge$ With external capacitor of 10 nF

of input. Choosing source node as the integrating node, filters with high linearity can be realized. Therefore, filters based on source followers are explored in the next part of the research. A second-order low pass Butterworth filter based on source follower is proposed. The main idea is to exploit the strengths of sub-threshold source follower circuit, like low noise, low output impedance, high linearity and low power. Switching technique is also adopted to the filter where in the transistor bias currents are switched to enable the bandwidth tuning. A PTAT current reference circuit is designed to keep the bandwidth intact across process, voltage and temperature variations. This filter offers a very high dynamic range up to 91 dB and consumes power as low as 25 nW making it one of the energy efficient designs.

The proposed resistor based tuning (R-tuning), used in the first filter adopting g_m reduction, has a limited tuning range. The reason is the following. When the g_m is reduced using R-tuning, the output impedance of the transcondcutor does not scale. Therefore, beyond a certain point output conductance of the transconductor dominates over g_m resulting bandwidth saturation. Another impact is the reduction in the filter DC gain. A scheme to enhance the output resistance of a differential amplifier is proposed. A negative resistance is used to cancel the output resistance of the differential amplifier. This inturn is achieved through a transimpedance based loop. It is proved that the proposed scheme can give a gain enhancement of about two folds (in dB) compared to the gain of basic differential transconductor, without loss in linearity. An OTA designed using this scheme is found to offer least sensitivity of gain boost over output voltage swing across process corners, at nominal voltage and temperature, when compared to other methods found in literature. First order filter is designed using the r_o enhanced OTA. With the gain enhanced OTA, it is able to reduce the cut-off frequency further, without the loss of DC gain.

In bio-medical filters, the pass band gain of the filters should be constant, in order to preserve the useful information embedded in the morphology of the filtered signal Neshatvar (2010), so Butterworth filters are preferred compared to other filter topologies. Accordingly, in this thesis, all filters are designed to offer Butterworth response. The proposed architectures are designed in 0.18 μm standard CMOS process and targeted for operation on a supply voltage of 1.8 V. The transistors are operated in weak inversion region to achieve low power consumption.

1.4 Thesis Organization

In Chapter 1, after a brief introduction about biomedical signals, a detailed discussion on motivation behind choosing this topic is presented. Also, a detailed review on various filter techniques used in filtering biomedical signals along with their limitations is presented.

Chapter 2 presents a novel scheme for realizing low bandwidth filters. The scheme is validated through a fourth-order, low pass Butterworth transconductor capacitor (g_m-C) filter with tunable bandwidth for biomedical signal processing front-ends. Two bandwidth tuning schemes have been proposed for the filter.

Chapter 3 presents a second-order low pass Butterworth filter based on a sub-threshold source follower bi-quads. It also outlines the switching technique adopted for the filter where in the transistor bias currents are switched, to enable the bandwidth tuning.

In Chapter 4, a scheme to enhance the output resistance of a differential amplifier is presented. It explains the scheme in detail where a gyrator based loop is used to offer a negative resistance to cancel the output resistance of the differential amplifier. It then presents a first order low-pass filter designed using the enhanced OTA.

The thesis is concluded in Chapter 5 throwing highlights on possible future works.

Chapter 2

DESIGN OF LOW FREQUENCY LOW PASS g_m-C FILTER

2.1 Introduction

The main objective of this research is to propose low power low frequency filters and validate by designing such filters. g_m-C filter topology is chosen for the reasons outlined in Chapter 1. In bio-medical electronics, filters with tunable bandwidth, that extracts most bio potential signals are widely preferred to enhance the re-usability of the filter and for cost minimization. Also, the main focus in design of such filters is to minimize the power and area of the designed filter circuits. In this chapter a novel technique for realizing transconductors for low frequency filters has been presented. The main source of power loss in such filters is the transistor loss. Therefore, to minimize the amount of power lost in the circuit, the transistors are operated in weak inversion region by biasing them with low quiescent currents. However, this comes at a cost in-terms of noise and mismatch.

Using the proposed transconductor architecture two fourth order tunable low-pass filters have been designed to prove the candidature of the proposed transcondutor. With a careful design, the effect of mismatch has been kept sufficiently low. These filters are capable of handling different bio potential signals such as ECG, EEG and EMG.

The specifications are chosen to be same for both the filters and are outlined below.

- Filter response type : Butterworth
- Filter order (N) : 4
- 3-dB bandwidth (f_c) : Tunable upto 100 Hz
- Filter realization : Cascade of biquads
- Architecture : g_m-C
- Supply voltage (V_{DD}) : 1.8 V
- Technology : 0.18 μm CMOS process from UMC Technologies

2.2 Proposed Transconductor Architecture

A transconductor is voltage controlled current source where the output current is proportional to input voltage (single ended or differential) and the constant of proportionality is called as 'transconductance'. A symbolic representation of a fully differential transconductor is shown in Figure 2.1.

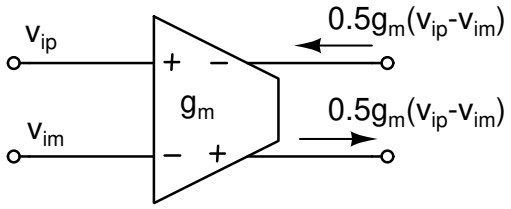


Figure 2.1: Symbol of a fully differential transconductor.

$$i_o = 0.5 g_m \left(v_{ip} - v_{im} \right) \tag{2.1}$$

In a fully-differential system, typically it is expected that $v_{ip} = -v_{im}$.

The requirement on realizing low frequency filters is that the transconductance should be kept small enough to keep the bandwidth at a desired value, sub-hundred hertz.

A novel technique has been proposed for designing a low valued transconductor. The proposed scheme is presented in Figure 2.2. Two simple source-coupled differential pairs formed using transistors M_1, M_4 and M_2, M_3 form the basic low g_m transconductor. All the transistors are sized equal. The two differential pairs are biased with different tail currents I_{SS1} and I_{SS2}. The tail currents are chosen such that

$I_{ss1} \approx I_{ss2}$ and $I_{ss1} - I_{ss2} = \Delta i$. The cross coupled arrangement of the two differential pairs effectively offers a low transconductance and is explained as follows.

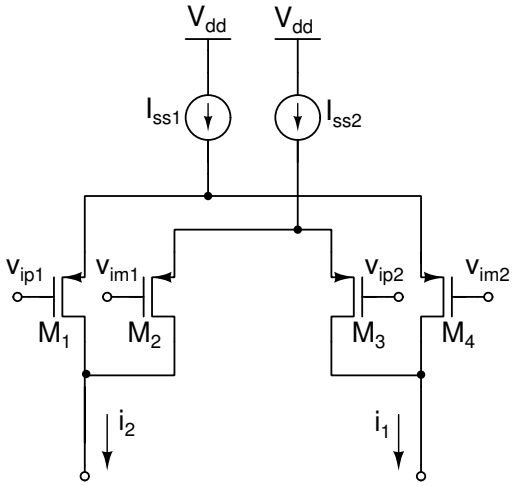


Figure 2.2: Cross-coupled differential pair.

Let, g_{m1}, g_{m2} be the transconductances of $M_{1,4}$ and $M_{2,3}$ respectively due to the currents $I_{SS1}/2$ and $I_{SS2}/2$ flowing through them. The differential component of small signal output currents i_1 and i_2 can be written as in (2.2) and (2.3).

$$i_1 = 0.5\, g_{m1}(v_{ip1} - v_{im2}) + 0.5\, g_{m2}(v_{im1} - v_{ip2}) \tag{2.2}$$

$$i_2 = -i_1 \tag{2.3}$$

If $v_{ip1} = v_{ip2} = v_{ip}$ and $v_{im1} = v_{im2} = v_{im}$, for differential operation with $v_{ip} = -v_{im}$, (2.2) can be rewritten as

$$\begin{aligned} i_1 &= g_{m1} v_{ip} - g_{m2} v_{ip} \\ &= (g_{m1} - g_{m2})\, v_{ip} \end{aligned} \tag{2.4}$$

Defining $g_{m,eff} = g_{m1} - g_{m2}$ as effective low output transconductance, i_1 and i_2 can be written as

$$i_1 = g_{m,eff}\, v_{ip} \tag{2.5}$$

$$i_2 = -g_{m,eff}\, v_{ip} = g_{m,eff}\, v_{im} \tag{2.6}$$

The transistors are operated in weak inversion so has to achieve nano-amperes of bias current and hence the lower power. For the given drain current g_m of transistor in weak inversion is higher than in saturation. However, with nano-amperes of drain current, the transistors is invariably operated in weak inversion. This also helps in reducing $g_{m,eff}$.

For transistors operated in weak-inversion, the transconductance is given by $g_m = \frac{I_D}{\eta V_T}$ where I_D is the drain current, η is the sub-threshold slope factor and V_T is the thermal voltage. A detailed discussion on this has been presented in Appendix A-7

With operation in weak-inversion, $g_{m,eff}$ can be written as

$$\begin{aligned} g_{m,eff} &= g_{m1} - g_{m2} \\ &= \frac{I_{ss1}}{2\,\eta V_T} - \frac{I_{ss2}}{2\,\eta V_T} \\ &= \frac{\Delta i}{2\,\eta V_T} \end{aligned} \tag{2.7}$$

It is evident from (2.7) that, $g_{m,eff}$ is a function of Δi. Therefore, the transconductance can be made small and tuned to the bandwidth requirement of the filter by tuning Δi, the difference between I_{ss1} and I_{ss2}. A scheme to generate tail currents I_{ss1} and I_{ss2} with a tunable difference is proposed and presented.

2.2.1 Tunable Tail Current Generation

To achieve low transconductance, the two currents I_{ss1} and I_{ss2} are to be generated such a way that they have a very small difference Δi. And for tuning the bandwidth, Δi should be made adjustable. The circuit proposed here is capable of serving both the requirements. The proposed circuit is shown in Figure 2.3. It consists of a simple source-coupled differential pair ($M_{x1} - M_{x2}$) with inputs V_x and V_y. $M_{x4,5}$ operate in near sub-threshold and current density of M_{x5} is maintained equal to M_{x1} and M_{x2}, current density of Mx4 is maintained equal to M_{x1}.

Drain currents of M_{x1} and M_{x2} are mirrored as tail currents I_{ss1} and I_{ss2} respectively with a mirroring ratio 'k'. Then, the Δi can be defined as,

$$\Delta i = k\, g_{m,x}(V_x - V_y) \tag{2.8}$$

where, $g_{m,x}$ is the transconductance of transistor M_{x1}(and M_{x2}). The potential difference V_{xy} is generated from voltage drop across a tunable resistor R such that $V_{xy} = I_b R$. With this setup, the effective transconductance of the main transconductor can be written as in (2.10)

$$g_{m,eff} = \frac{\Delta i}{2\,\eta V_T} \tag{2.9}$$

$$= \frac{k\,g_{m,x} I_b R}{2\,\eta V_T} \tag{2.10}$$

$$g_{m,eff} = \frac{k\,I_b^2 R}{4\,(\eta V_T)^2} \tag{2.11}$$

The transconductor can be tuned by either tuning the resistance R or I_b. However, R tuning is preferred because of linear relation with $g_{m,eff}$ and hence the bandwidth. The diode connected transistors M_{x4} and M_{x5} set the common-mode bias for the differential pair.

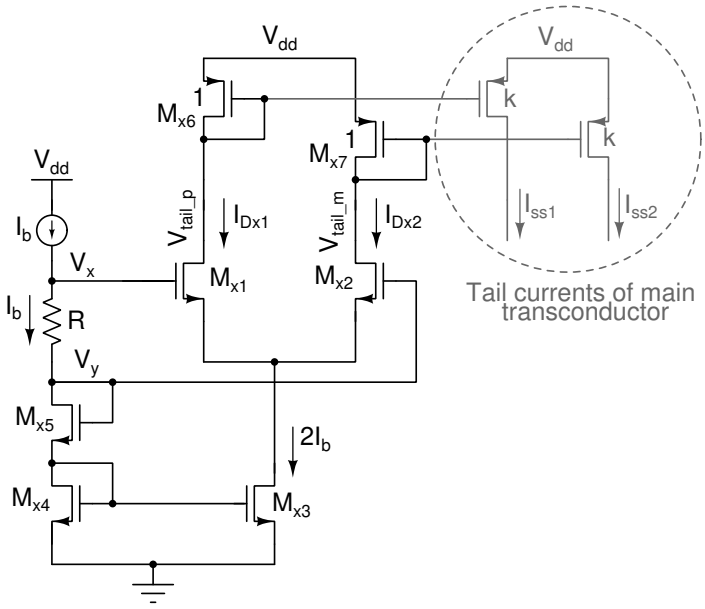


Figure 2.3: Tunable tail current generation circuit.

2.3 Filter Realization - Proposed Architecture

Using the proposed transconductor, an architecture for realizing a fully-differential filter without the need for explicit CMFB circuits is proposed. The architecture is explained with the help of first order filter.

2.3.1 First Order Filter

A common architecture used for realizing a first order fully differential low-pass g_m-C filter is shown in the Figure 2.4.

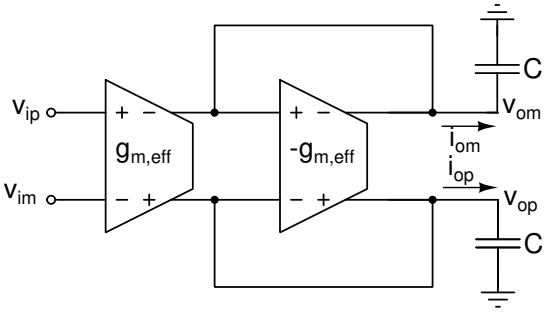


Figure 2.4: First-order fully differential g_m-C filter.

The first order filter can also be realized using a differential-in single-ended-out transconductors, in which case one must be using pseudo-differential architecture. Schematic of such a filter is shown in Figure 2.5

For filters in both Figure 2.4 and Figure 2.5, the transfer function is given in (2.12)

$$\frac{v_{op} - v_{om}}{v_{ip} - v_{im}} = \frac{1}{1 + \frac{s}{\omega_o}} \tag{2.12}$$

where, $\omega_o = \frac{g_{m,eff}}{C}$ is the filter bandwidth.

Comparing the two filter architectures, the former requires a CMFB circuit to maintain the output common-mode DC voltage to the desired value, commonly preferred to be same as that of the input common-mode DC when realizing higher order filters using cascade of sections. The issues related to the design of good common-mode feedback (CMFB) circuit presented in Choksi and Carley (2003) are, the unity gain bandwidth and slew rate of the CMFB circuit must be comparable to that of transconductor to avoid output distortion. The gain of the CMFB circuit must be

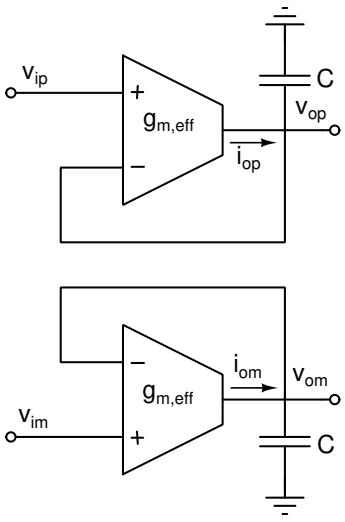


Figure 2.5: First-order pseudo differential g_m-C filter using differential-in single-ended-out transconductors.

large enough to accurately set the common-mode voltage. For good stability, the CMFB circuit should be compensated for better phase margin and fast settling step response. The other drawback is a n^{th} order fully differential filter requires n CMFB circuits, demanding additional area, power and circuit complexity. However, with the differential input signal, the common-mode range requirement for the differential-pair of the input stage is quite relaxed.

In contrast, the pseudo differential filter in Figure 2.5 does not require any explicit CMFB circuit. The feedback ensures that the output common-mode DC is almost equal to the input common-mode. But, the same feedback demands a large common-mode range for the differential-pair of the input stage.

We propose a method to realize a fully differential filter using the proposed transconductor that neither demands for explicit CMFB circuits nor it demands wide common-mode range.

2.3.2 Proposed Filter Realization Scheme

First, the pseudo-differential version of the first order filter shown in Figure 2.5 has been realized using the proposed low-g_m transconductor cell. The scheme of realization is shown in Figure 2.6a and is explained as follows.

The g_m cell along with a NMOS current mirror load provides a single ended output.

Two such arrangements (leg-1 and leg-2 in figure) together provide pseudo-differential output. For leg-1, the transconductor inputs v_{ip2} and v_{im2} are drawn from v_{om} and v_{op} of the differential output. Whereas v_{ip1} and v_{im1} are fed with inputs v_{ip} and v_{im}. From (2.2), the output currents i_1 and i_2 can be written as

$$\begin{aligned} i_1 &= 0.5\, g_{m1}(v_{ip} - v_{op}) + 0.5\, g_{m2}(v_{im} - v_{om}) && (2.13) \\ i_2 &= -i_1 && (2.14) \end{aligned}$$

From (2.13) and (2.14), the output current $i_{op} = i_1 - i_2$ can be written as

$$\begin{aligned} i_{op} &= i_1 - i_2 \\ &= g_{m1}(v_{ip} - v_{op}) + g_{m2}(v_{im} - v_{om}) && (2.15) \end{aligned}$$

For differential operation with $v_{ip} = -v_{im}$ and $v_{op} = -v_{om}$, (2.15) can be rewritten as

$$\begin{aligned} i_{op} &= (g_{m1} - g_{m2})(v_{ip} - v_{op}) \\ &= g_{m,eff}(v_{ip} - v_{op}) && (2.16) \end{aligned}$$

The leg-2, provides i_{om}, and is derived by interchanging v_{ip} with v_{im} and v_{op} with v_{om} at the input terminals of g_m-cell. Thus, the output current i_{om} can be written as,

$$i_{om} = g_{m,eff}(v_{im} - v_{om}) \tag{2.17}$$

The transfer function of this filter can be derived as,

$$\begin{aligned} v_{op} &= i_{op} \cdot \frac{1}{sC} = g_{m,eff}(v_{ip} - v_{op}) \cdot \frac{1}{sC} \\ v_{om} &= g_{m,eff}(v_{im} - v_{om}) \cdot \frac{1}{sC} && (2.18) \\ v_{op} - v_{om} &= \frac{g_{m,eff} \cdot 1/sC}{1 + g_{m,eff} \cdot 1/sC} \cdot (v_{ip} - v_{im}) \\ \frac{v_{op} - v_{om}}{v_{ip} - v_{im}} &= \frac{1}{1 + \frac{sC}{g_{m,eff}}} && (2.19) \end{aligned}$$

The resulting transfer function $\frac{v_{op}-v_{om}}{v_{ip}-v_{im}}$ takes the form given in (2.12). Note that, because of feedback, the output common-mode is set equal to the input, provided the DC gain is sufficiently large. However, the proposed arrangement is limited by

common-mode range requirement. This is due to the fact that the common-source nodes ($A1$ and $A2$ in leg-1; B_1 and B_2 in leg-2) experience a large signal swing for in-band frequencies and therefore they are no-longer at small signal ground. For example, the swing at node A_1 is influenced by v_{ip} and v_{op}, and both v_{ip} and v_{op} are swinging almost equal for in-band frequencies. A careful look at the two legs reveal that nodes A_1 and B_1 (similarly, node A_2 and B_2) experience equal but opposite signal excursions. Joining these nodes will force the nodes to small-signal ground, thus offering a fully-differential version of the filter. This modification has been shown by dotted lines in Figure 2.6a. This is not the case with the simple cross coupled differential pair shown in Figure 2.2. The common-source nodes here is not at small-signal ground (the two inputs are not differential) and there is going to be a signal dependent common-mode voltage. Thus, the proposed architecture in Figure 2.6 has a better linearity when compared to Figure 2.2. The simplified schematic of the fully differential first order block is shown in Figure 2.6b.

The transistor sizes for the proposed filter with the biasing circuit, designed in 0.18 μm CMOS process from UMC Technologies, are listed in Table 3.1.

Table 2.1: Transistor sizes of the proposed filter and biasing circuit

Transistor	N(W/L)
M_{1-4}, M_{7-10}	2 (0.25/48)
$M_{5,6}$, $M_{11,12}$	2 (2/48)
$M_{x1,x2}$	2 (1/48)
M_{x3-x5}	2 (2/48)
$M_{x6,\,x7}$	2 (2/48)
Mirroring ratio $k = 1$	

Where N is the number of fingers and
W, L are width and length of the transistors in μm.

The gate length (L) of the transistors are kept much higher than the width (W) for the following two reasons.

1. To maintain sufficiently large output resistance of the filter so as to get a decent DC gain.
2. To reduce gm of each transistor so that the effective transconductance ($g_{m1} - g_{m2}$) is made sufficiently small.

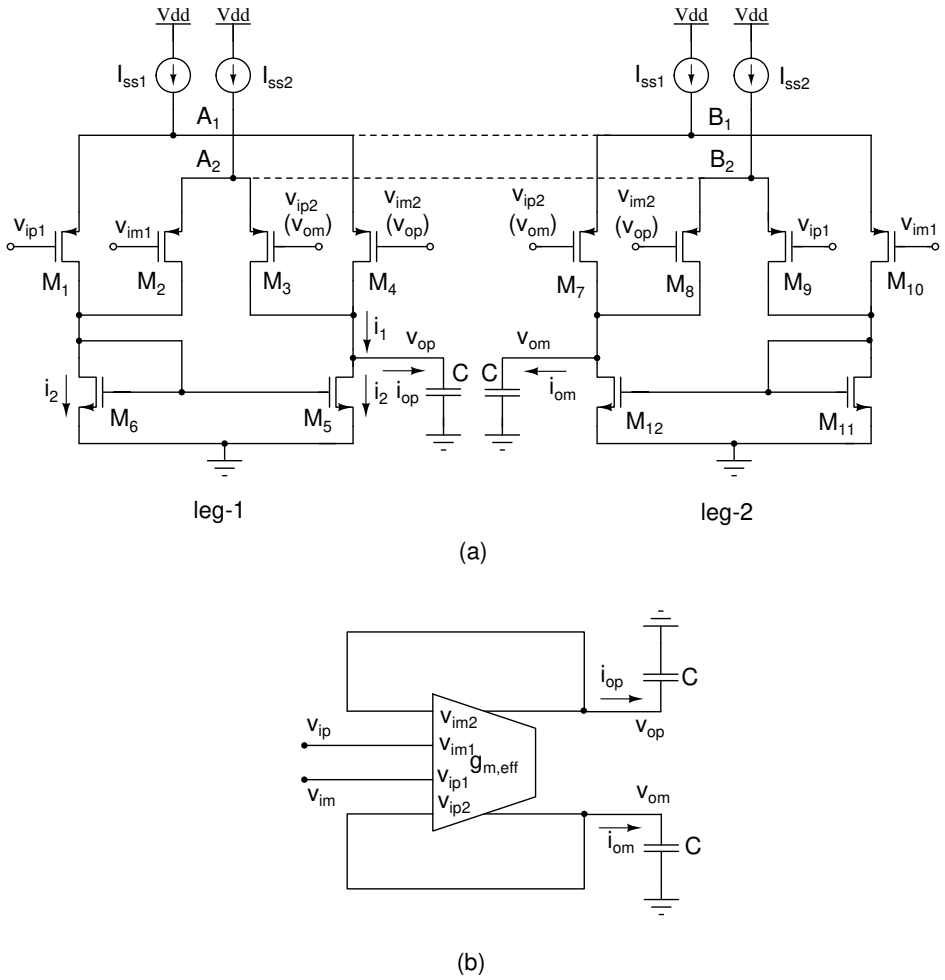


Figure 2.6: (a). Complete schematic of differential first order g_m-C filter (b). Simplified schematic of the fully differential first order block

Usage of large L for all transistors also helps to increase the output resistance of transistors and thus to achieve accurate current mirroring. In addition, the resulting large gate area helps in minimizing the effect of mismatches and the dominant flicker noise (Razavi 2005).

2.3.2.1 Noise Analysis

The noise model of differential first order g_m-C filter is shown in Figure 2.7. For noise analysis, both flicker noise and thermal noise are considered.

The total output noise current $i_{op,n}$, due to noise currents of the transistors $M_1 - M_6$

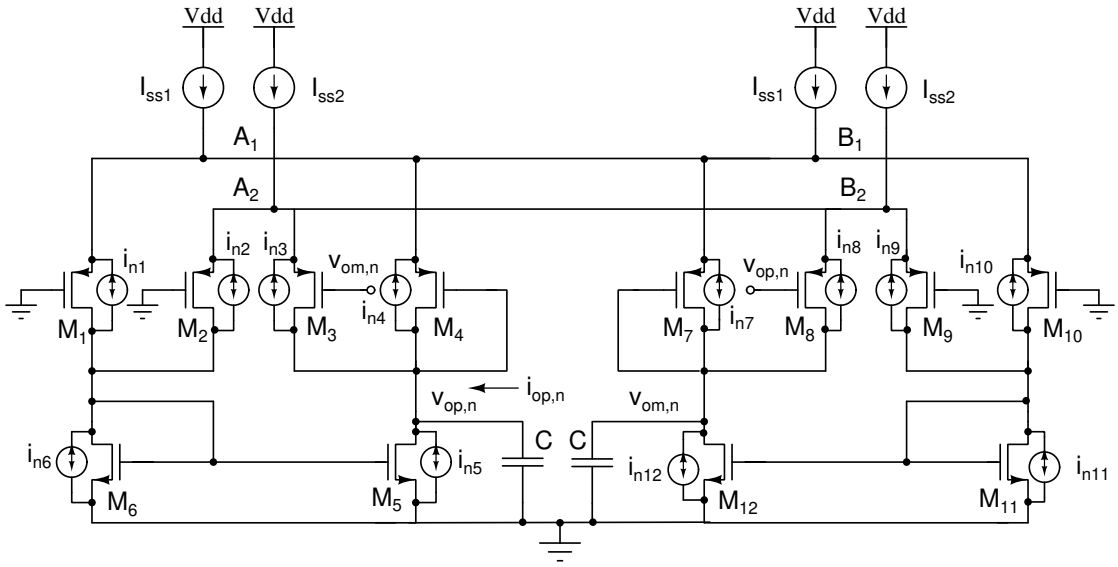


Figure 2.7: Equivalent noise model of differential first order g_m-C filter used for analysis.

is given by,

$$i_{op,n} = -(i_{n1} + i_{n2} + i_{n3} + i_{n4} + i_{n5} + i_{n6}) \tag{2.20}$$

The impedance looking into the output node is given by,

$$r_{op,eq} = \frac{1}{(g_{m4} - g_{m3}) + g_{o3} + g_{o4} + g_{o5}} \tag{2.21}$$

The total output voltage noise is,

$$\begin{aligned} V_{op,n} &= -i_{op,n} r_{op,eq} && (2.22) \\ &= -(i_{n1} + i_{n2} + i_{n3} + i_{n4} + i_{n5} + i_{n6}) \\ &\quad \times \frac{1}{(g_{m4} - g_{m3}) + g_{o3} + g_{o4} + g_{o5}} && (2.23) \end{aligned}$$

The mean-squared noise over 1 Hz is given by

$$\begin{aligned} \overline{V_{op,n}^2} &= 4kT\gamma \frac{(2g_{m1} + 2g_{m2} + g_{m5} + g_{m6})}{(g_{m1} - g_{m2})^2} \\ &\quad + \frac{K_F}{C_{ox} W L f} \frac{[2g_{m1}^2 + 2g_{m2}^2 + g_{m5}^2 + g_{m6}^2]}{(g_{m1} - g_{m2})^2} \end{aligned} \tag{2.24}$$

2.4 Fourth Order Low Pass Filter

A fourth-order low-pass Butterworth filter has been realized as cascade of second-order filters. The second order filter is implemented by using an architecture whose single ended version is shown in Figure 2.8(Chang 1999).

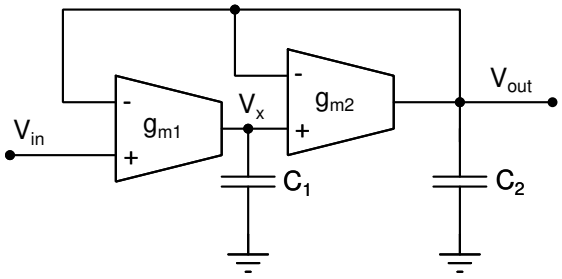


Figure 2.8: Single ended second order low-pass g_m-C filter.

This architecture for realizing the second order filter perfectly suits the approach proposed in the previous section.

$$V_{out} = \frac{g_{m2}}{sC_2}\left(V_x - V_{out}\right) \tag{2.25}$$

$$V_x = \frac{g_{m1}}{sC_1}\left(V_{in} - V_{out}\right) \tag{2.26}$$

The transfer function of the filter in Figure 2.8 is given by,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + \left(\frac{g_{m2}}{C_2}\right)s + \frac{g_{m1}g_{m2}}{C_1C_2}} \tag{2.27}$$

where g_{m1}, g_{m2} are the transconductances and C_1, C_2 are the integrating capacitances. Comparing (2.27) with the transfer function of second order low pass filter prototype given by (2.28), the pole-frequency ω_p and the quality factor Q of the filter can be written respectively as in (2.31) and (2.30)

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\omega_p^2}{s^2 + \left(\frac{\omega_p}{Q}\right)s + \omega_p^2} \tag{2.28}$$

$$\omega_p = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{2.29}$$

$$Q = \sqrt{\frac{g_{m1}C_2}{g_{m2}C_1}} \tag{2.30}$$

If the transconductors are assumed to have same transconductance, say g_m, expression for ω_p and Q reduces to

$$\omega_p = \frac{g_m}{\sqrt{C_1 C_2}} \tag{2.31}$$

$$Q = \sqrt{\left(\frac{C_2}{C_1}\right)} \tag{2.32}$$

Schematic of the fully-differential fourth order Butterworth low-pass filter realized using the proposed transconductor is shown in Figure 2.9. The value of Q for each second order section in the filter is taken from the filter table (Van Valkenburg and Shaumann 2001). For a given $g_{m,eff}$=2 nS and for Q values from the filter table, the integrating capacitances for each second order section are computed using the equations (2.31) and (2.32) and is shown in Table 2.2.

Table 2.2: Integrating capacitances for fourth order filter.

	Capacitor	**Value (pF)**
$Q = 0.541$	C_1	58.99
	C_2	17.27
$Q = 1.306$	C_3	24.42
	C_4	41.72

2.4.1 Simulation Results

The g_m reduction scheme is validated through a fourth order Butterworth low-pass filter designed in 0.18 μm CMOS from UMC technologies. The filter is designed to have a tuning range from 1 Hz to 100 Hz. All the transistors are designed to operate in sub threshold region. For the given transconductance of 2 nS and bandwidth of 100 Hz,

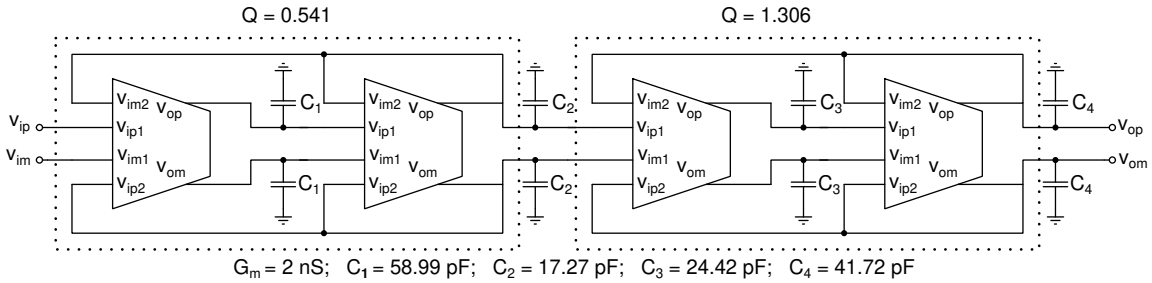


Figure 2.9: Fully differential fourth order filter.

the intended capacitances for each second order section are computed. Figure 2.10

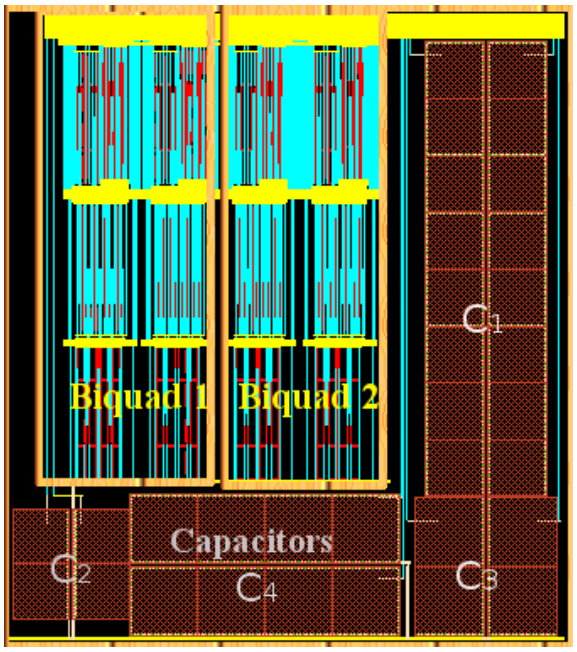


Figure 2.10: Layout of the proposed fourth order fully differential low-pass filter with biasing circuit.

shows the layout for fully differential fourth order filter shown in Figure 2.9. The total layout area is 0.91 mm × 0.81 mm. Due to the large size of transistors, the transistor and layout parasitic need to be accounted for. Therefore, the integrating capacitors are tuned to account for the parasitic capacitance at all four integrating nodes.

The maximum value of tuning resistor R is taken to be the value giving an effective transconductance of 2 nS for the transconductor. The resistor R is tuned to vary the bandwidth. The magnitude response of the filter for R tuning is shown in the

Figure 2.11. In Figure 2.12 bandwidth f_c as function of resistor R is plotted. It can be clearly seen that, f_c is fairly a linear function of R. An off-chip resistor (potentiometer) is preferred for R, over on-chip resistor, for the ease of tuning.

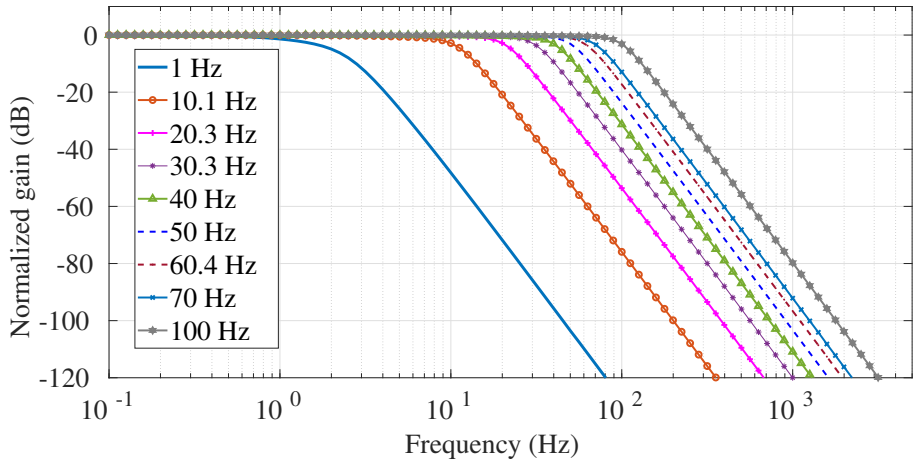


Figure 2.11: Magnitude response of the filter for R tuning.

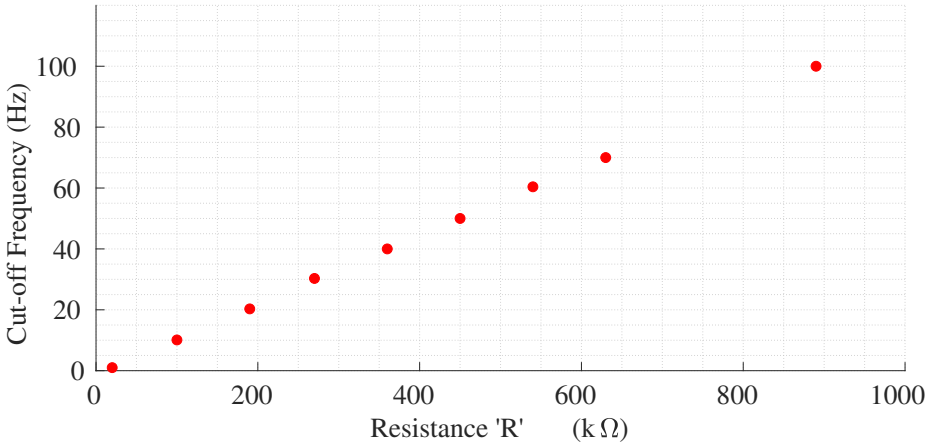


Figure 2.12: Tuning graph showing f_c for different values of R.

Monte-Carlo simulation has been carried out to check the robustness of the design against process mismatches. Figure 2.13 shows the distribution of f_c for 100 samples when the R is set for f_c=50 Hz. The mean is found to be 49.36 Hz and standard deviation is about 1.9 Hz. The output referred noise of the filter for 50 Hz setting is plotted in Figure 2.14. It is seen noise below 1 Hz is dominated by flicker noise. The

corner frequency is found to be about 0.8 Hz. The rms input referred noise integrated over 100 mHz - 100 Hz is found to be 109 μV for 50 Hz bandwidth setting.

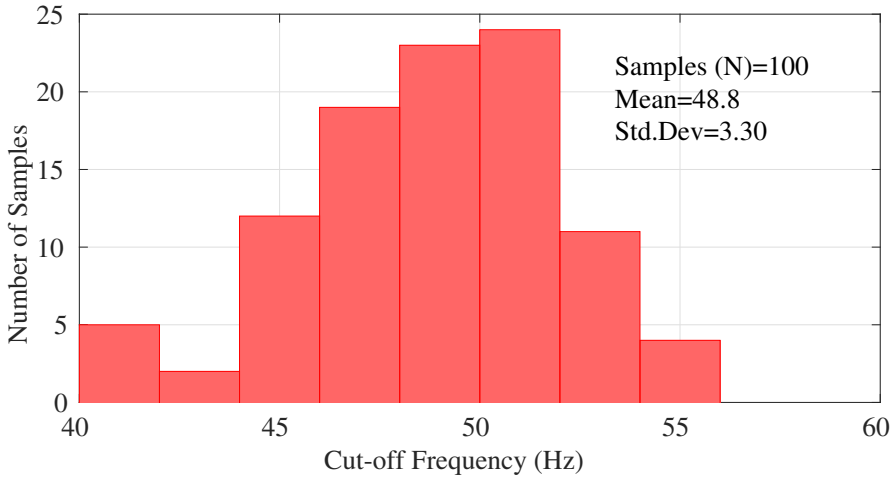


Figure 2.13: Monte-carlo simulation of the filter with 100 runs for f_c=50 Hz setting.

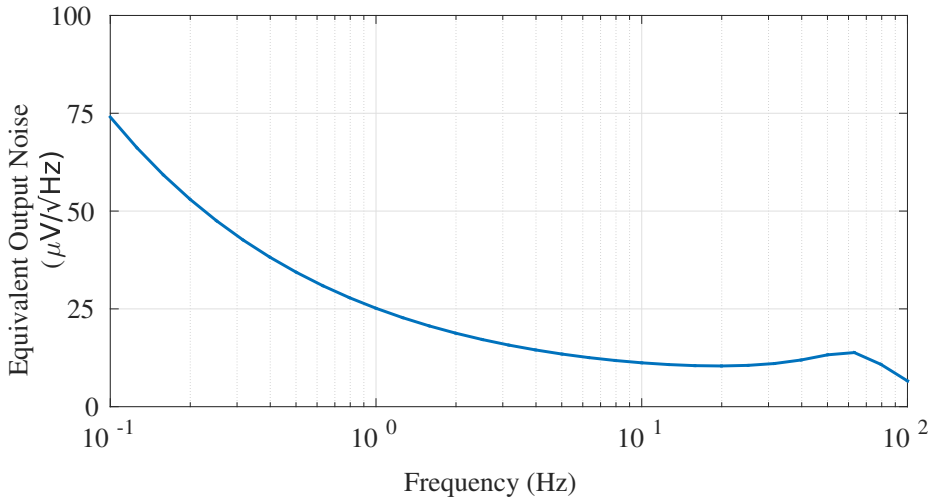


Figure 2.14: Output referred noise of the filter.

Simulations are carried out for variations across process corners, supply voltage and temperature (PVT), for a bandwidth setting of 50 Hz. The magnitude response of the filter at various process corners is shown in Figure 3.15. It is observed that the change in bandwidth is less than 10 % at nominal supply voltage of 1.8 V and at room temperature (27°C). Figure 3.17 shows the magnitude response for variation in

temperature from 0°C to 80°C at typical corner and nominal supply voltage. The change in bandwidth is less than 12 %. For the ±10% variation in supply voltage from the nominal value at room temperature and at typical process corner, the change in bandwidth observed is less than 1 % as shown in the Figure 3.16. These deviations can be tuned back by re-adjusting R appropriately. The efficiency of the proposed

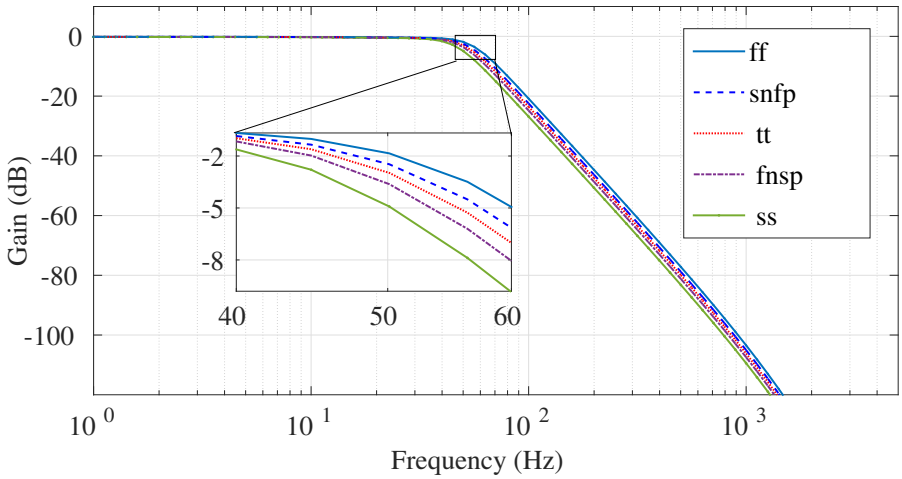


Figure 2.15: Magnitude response of the filter across various process corners at room temperature.

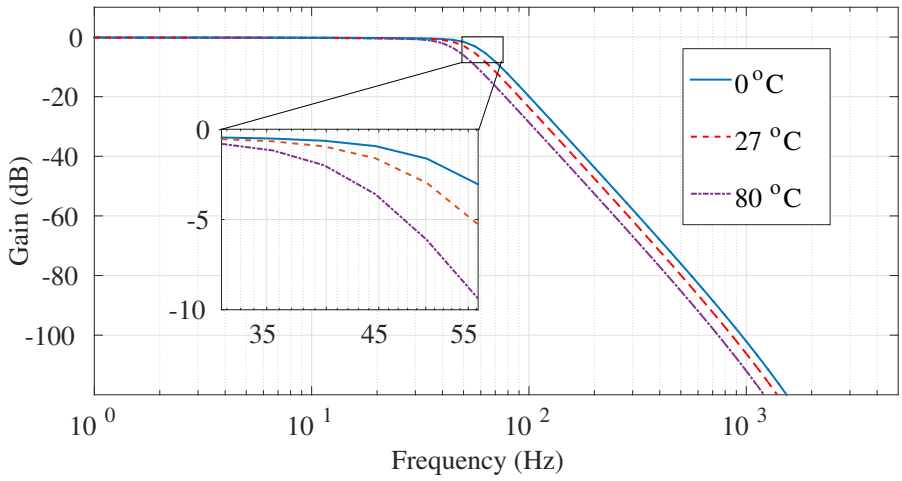


Figure 2.16: Magnitude response of the filter for change in temperature $(0 - 80^{o}\text{C})$ at typical corner and nominal supply voltage (V_{DD}=1.8 V).

filter is illustrated by filtering the ECG signal. The noisy ECG signal shown in the

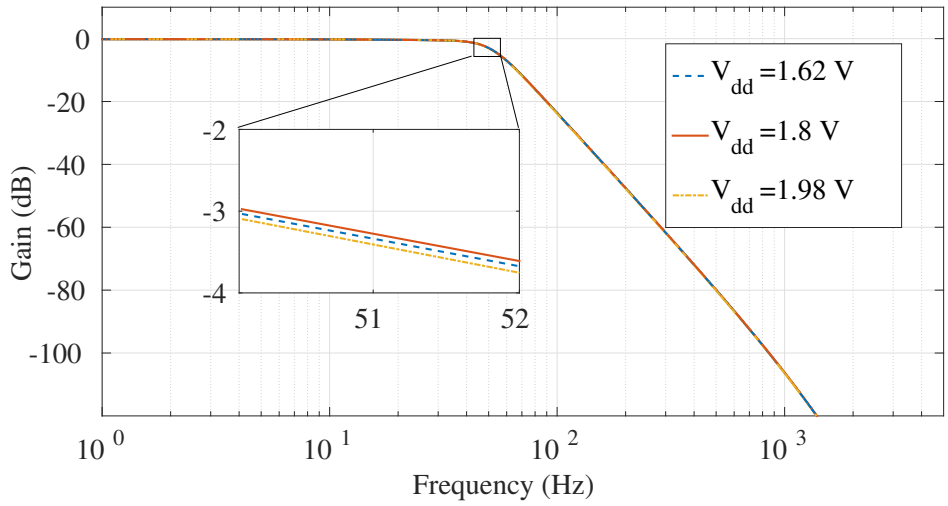


Figure 2.17: Magnitude response of the filter for 10% change in supply voltage at typical corner and room temperature.

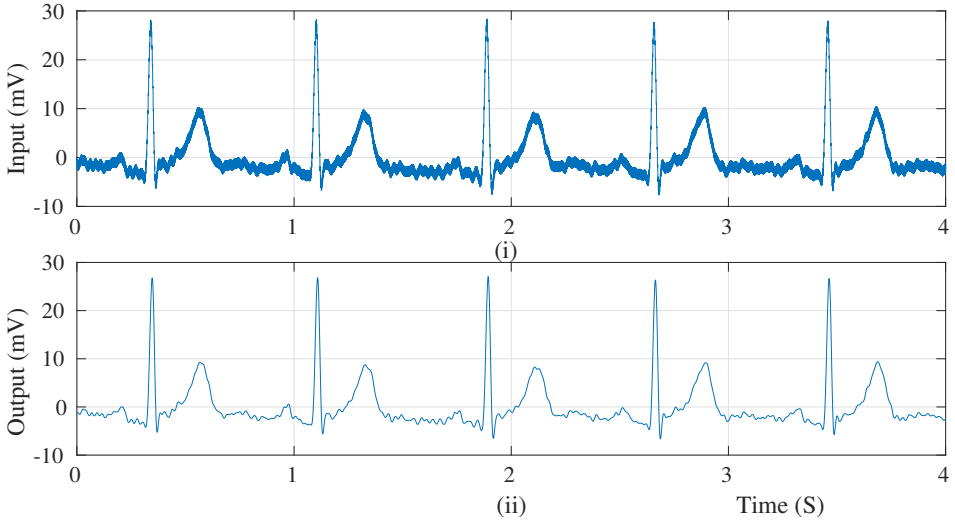


Figure 2.18: The post layout filter test for ECG:(i). The time representation of the original ECG signal (ii). The filtered ECG signal obtained from the proposed low pass filter (Normalized for DC gain).

Figure 2.18(i) is generated by adding an out-of-band noise (4 mV_pp, 500 Hz sinusoidal signal) to a pre-amplified original ECG signal obtained from Goldberger *et al.* (2000 (June 13). This noisy ECG signal is provided as an input to the proposed LPF with 100 Hz bandwidth. The output of the LPF is as shown in Figure 2.18(ii), and it is clearly visible that the out of band noise has been effectively filtered.

2.4.1.1 Limitations of the Filter

The proposed filter architecture suffer from the following limitations.

1. The filter bandwidth is decided by the ratio

$$\omega = \frac{g_{m,eff} + g_o}{C} \tag{2.33}$$

   When the $g_{m,eff}$ is reduced using R-tuning, the output impedance of the transconductor does not scale. Therefore, beyond a certain point the output conductance g_o of the transconductor dominates over $g_{m,eff}$ resulting in bandwidth saturation and also reducing the filter DC gain.

2. At low frequencies, the rms noise voltage increases almost by the factor by which the bandwidth is reduced. As can be seen in (2.24), tuning of R affects the effective transconductance $g_{m,eff}$ directly but the transconductance of individual transistors of the transconductors change marginally. The effect is that R tuning is fails to offer a good dynamic range at low bandwidth setting.

A method to mitigate the above mentioned limitations is to switch the output current of transconductor, flowing to the integrating capacitor, with a duty ratio D. This not only scales $g_{m,eff}$ by D but also g_o. The result is that the bandwidth changes with D without any bandwidth saturation and also the DC gain is maintained intact. With respect to the noise, the noise current from the transconductors flowing into capacitors is also scaled by D and therefore, the noise power remains constant with bandwidth scaling.

2.5 Switched Transconductor Filter

The switched transconductor based filter design approach is explained with the help of a first order g_m-C filter. In this approach the output current of the transconductor is switched with a specific D at a frequency sufficiently higher than the desired bandwidth. The effect is that the average current flowing into capacitor becomes a function of D, and hence reducing the effective g_m (Rodriguez-Villegas *et al.* 2011).

The basic principle of operation is shown in the Figure 2.19. Here a switch is employed to connect and disconnect the transconductor output from the load capacitor and feedback loop. The transconductor output current I_i flowing into the capacitor

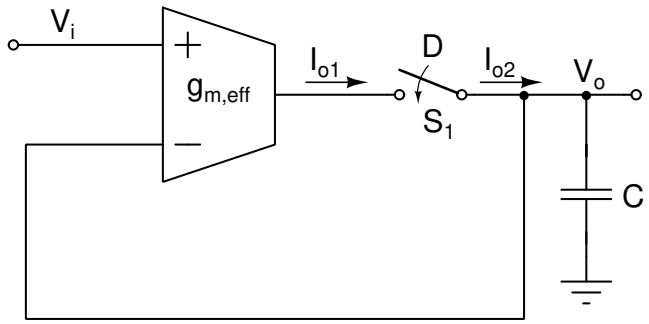


Figure 2.19: A switched g_m-C filter.

is dependent on the state of the switch. When switch S_1 is ON, the current I_i flows into the capacitor. When switch S_1 is OFF, the current flowing into the capacitor is zero. The use of switch S_1 reduces the average output current I_o that flows into the capacitor. If D is the duty ratio with which the switch S_1 is operated, then the average output current I_o given by (2.34). The effective transconductance of the switched transconductor denoted as $G_{m,eff}$ can be written as in (2.35).

$$I_{o2} = DI_{o1} \tag{2.34}$$

$$G_{m,eff} = Dg_{m,eff} \tag{2.35}$$

The transfer function for the switched transconductor filter shown in Figure 2.19 can be derived as follows. The output current can be expressed as,

$$I_{o2} = \begin{cases} g_{m,eff}V_i(s) - g_{m,eff}V_o(s) & 0 < t < T \\ 0 & T < t < T_s \end{cases} \tag{2.36}$$

If the signal is periodic with period T_s,

$$I_{o2}(s,t) = I_{o2}(s,t+T_s) \tag{2.37}$$

The output voltage is expressed as,

$$V_o(s,t) = I_{o2}(s,t)\frac{1}{sC} \tag{2.38}$$

If the output signal is considered periodic with period T_s,

$$V_o(s,t) = V_o(s,t+T_s) \tag{2.39}$$

Periodic signal can be represented as fourier series,

$$V_o(j\omega,t) = \sum_{k=-\infty}^{\infty} V_{o,k}(j\omega)\, e^{j(\omega+k\omega_s)t} \tag{2.40}$$

Where $V_{o,k}(j\omega)$ is given by,

$$V_{o,k}(j\omega) = \frac{1}{T_s}\int_0^{T_s} V_o(j\omega,t)\, e^{j\omega kt} dt \tag{2.41}$$

For k=0,

$$\begin{aligned} V_{o,0}(s=j\omega) &= \frac{1}{T_s}\int_0^{T_s} V_o(j\omega,t)\, dt \qquad (2.42)\\ &= \frac{1}{T_s}\int_0^{T} (g_{m,eff}V_i(j\omega) - g_{m,eff}V_o(j\omega))\frac{1}{j\omega C}\, dt + \int_T^{T_s} 0\, dt \\ V_o(j\omega) &= \frac{g_{m,eff}}{j\omega C}\left[V_i(j\omega) - V_o(j\omega)\right]\frac{T}{T_s} \qquad (2.43) \end{aligned}$$

Thus, the transfer function can be written as,

$$H(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{1}{1+\dfrac{j\omega C}{g_{m,eff}}\dfrac{T_s}{T}} \tag{2.44}$$

Defining, duty ratio $D = \frac{T}{T_s}$, The transfer function is given by,

$$H(s) = \frac{1}{1+\dfrac{sC}{Dg_{m,eff}}} \tag{2.45}$$

Actually, the diagram shown in Figure 2.19 doesn't satisfy the Kirchoff's current law when switch S_1 is OFF. There is no path for the current I_i to flow. This saturates the output of the transconductor near supply rails. To solve this, a dummy transconductor is required to create a path for the main transconductor when S_1 is off.

The second order filter architecture proposed in section 2.4 can be easily modified into a switched transconductor filter. Figure 2.20 shows the schematic of the proposed filter. Here, a switch is included between the output of the filter and capacitor. The phase ϕ of the clock, decides the duty ratio (D) of the switch and in this phase the integrating capacitors integrate the currents from the transconductors. During the phase $\overline{\phi}$, the transconductor currents are removed from capacitors and bypassed to transconductors dedicated for this purpose. This arrangement prevents the transconductor output from saturating. A fourth order filter is realized by cascading two sections.

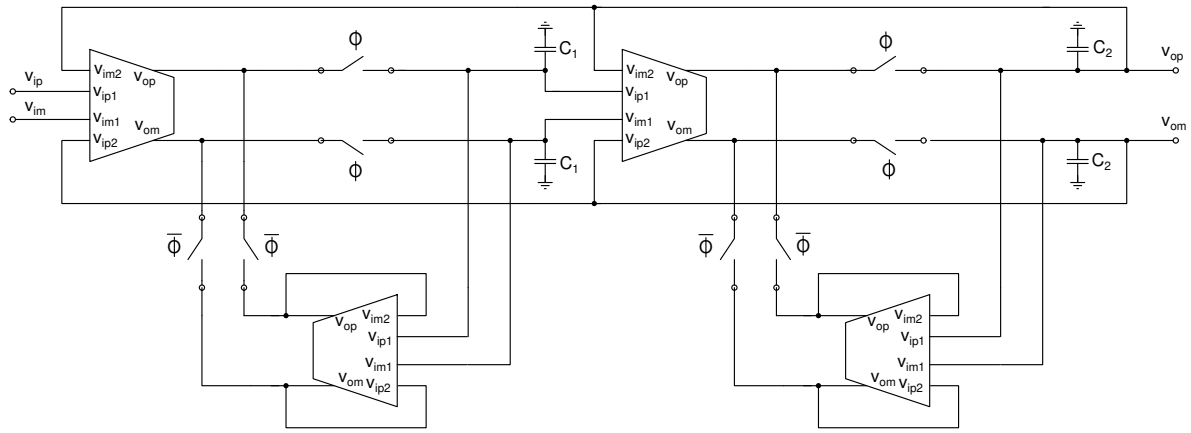


Figure 2.20: Fully differential switched second order filter.

2.5.1 Simulation Results

The proposed switched transconductor filter is validated through a fourth order Butterworth low-pass filter designed in 0.18 μm CMOS technology from UMC Technologies. The filter is designed to have a tuning range from 30 mHz to 100 Hz with the tuning resistor R set at value such that with D=100%, the bandwidth of the filter is 100 Hz. Figure 2.21 shows the layout of the filter. The total layout area is 1.34 mm $\times$ 0.93 mm. Figure 2.22 shows the magnitude response when D is varied from 0.01% to 100%. It is to be noted that, the clock frequency is adjusted accordingly to keep clock feed-through, if any, out of the stop-band frequency (corresponding to attenuation of 120 dB). The cutoff frequency is found to be adjustable from 30 mHz to 100 Hz. Tuning graph showing f_c as function of D is shown in Figure 2.23 proves that the tuning scheme is quite linear.

The output referred noise of the switched-g_m-C filter with D=50% (50 Hz bandwidth) is shown in the Figure 2.24. The rms value of the voltage noise integrated over the the band 100 mHz - 100 Hz is found to be 132.6 μV.

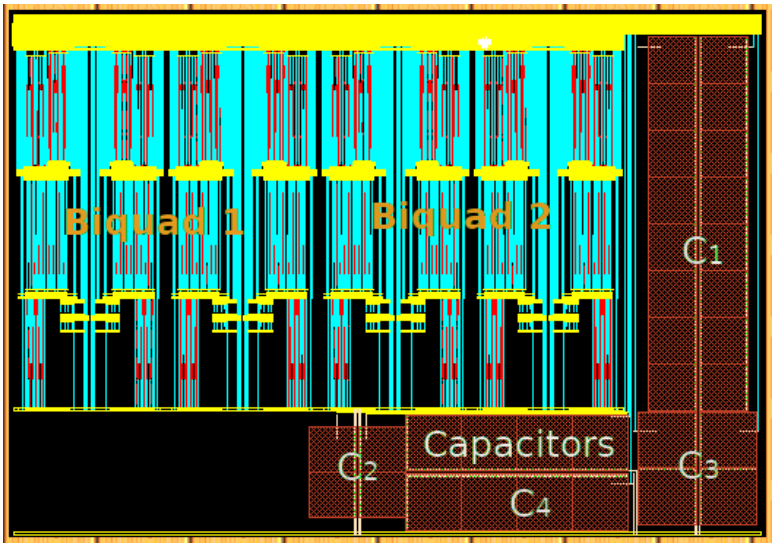


Figure 2.21: Layout of the proposed fully differential switched fourth order low-pass filter.

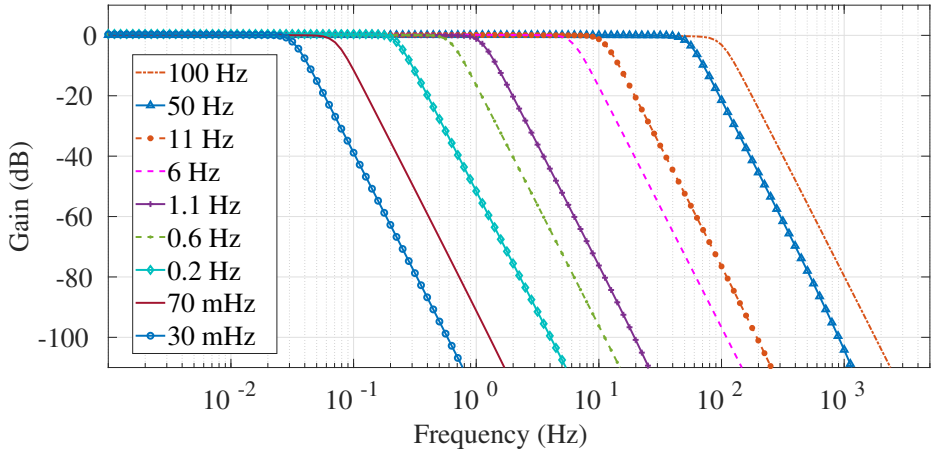


Figure 2.22: Magnitude response of the filter for duty ratio tuning.The tuning range is from 100 Hz to 30 mHz. The settings used for these results are in the format [clock frequency, duty cycle, cutoff frequency]: [10 kHz, 100%, 100 Hz], [5 kHz, 50%, 50 Hz], [1 kHz, 10%, 11 Hz], [1 kHz, 5%, 6 Hz], [100 Hz, 1%, 1.1 Hz], [100 Hz, 0.5%, 0.6 Hz], [100 Hz, 0.1%, 0.2 Hz], [10 Hz, 0.05%, 70 mHz] and [10 Hz, 0.01%, 30 mHz].

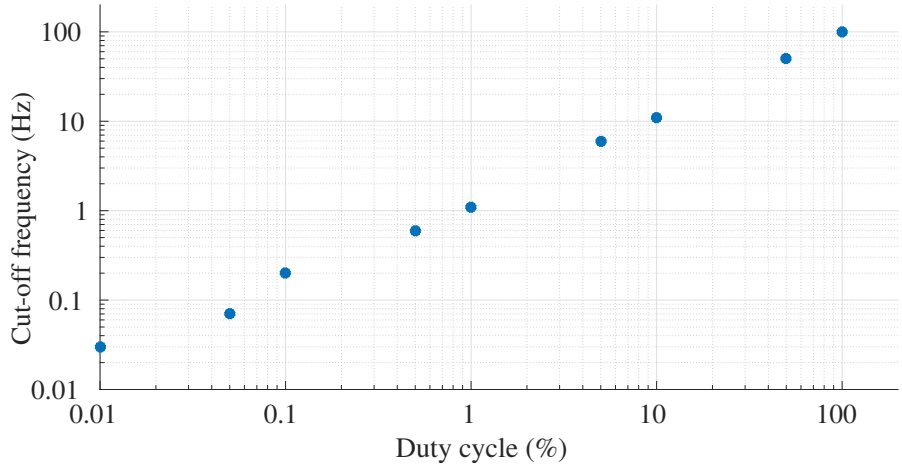


Figure 2.23: Tuning graph showing the filter cut-off frequency for different duty cycle.

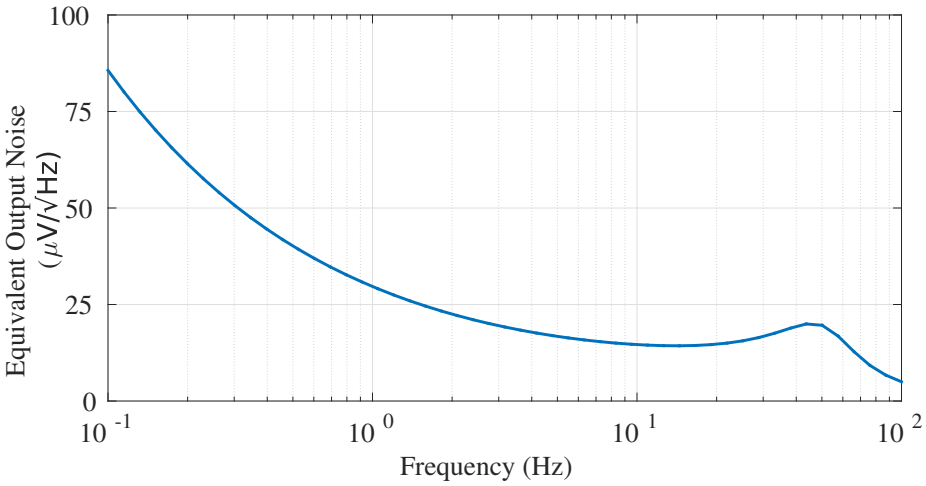


Figure 2.24: Output referred noise of the switched-g_m-C filter.

Simulations are carried out on the filter for variations across PVT, for a bandwidth setting of 50 Hz. The magnitude response of the filter at different process corners is shown in Figure 2.25. It is observed that the change in bandwidth is less than 10 % at nominal supply voltage of 1.8 V and room temperature (27°C). Figure 2.26 shows the magnitude response for variations in temperature from 0°C to 80°C at typical corner and nominal supply voltage. The change in bandwidth is less than 12 %. For the ±10% variation in supply voltage from the nominal value at room temperature and at typical process corner, the change in bandwidth observed is less than 1 % as shown

in the Figure 2.27. These deviations can be tuned back by re-adjusting the duty ratio D appropriately.

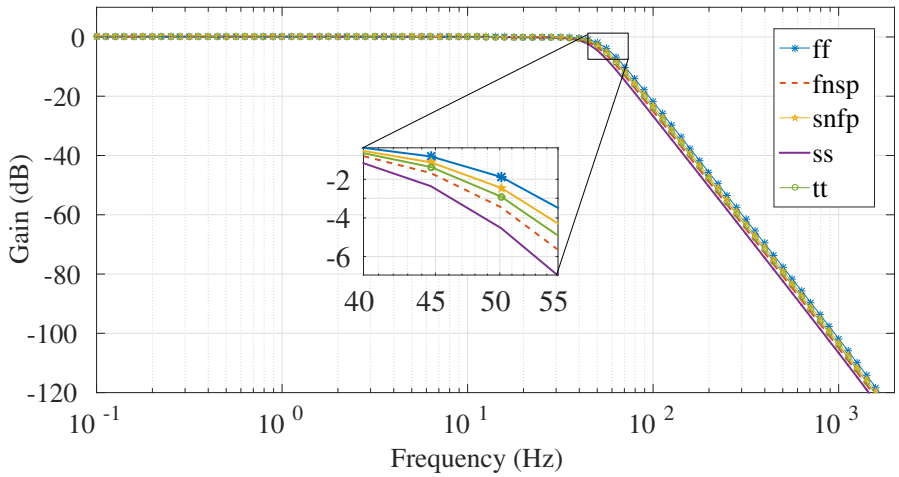


Figure 2.25: Magnitude response of the switched-g_m-C filter across various process corners at room temperature.

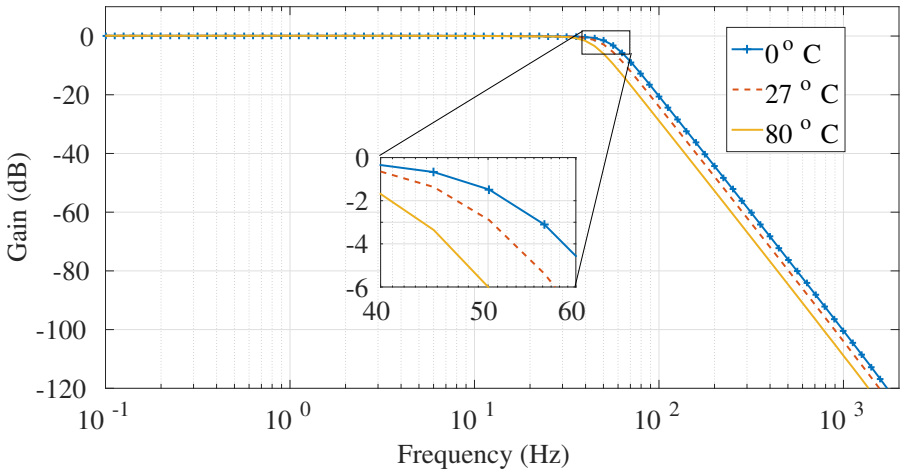


Figure 2.26: Magnitude response of the switched-g_m-C filter for change in temperature $(0 - 80^{o}\text{C})$ at typical corner and nominal supply voltage (V_{DD}=1.8 V).

The summary of performance of two filters, Filter-1 (with only R-tuning) and Filter-2 (with fixed-R and tuned D), is shown in Table 2.3.

For biomedical signal processing, being the main application of the proposed filters, flicker noise is one of the important parameter of concern. Flicker noise of a transistor

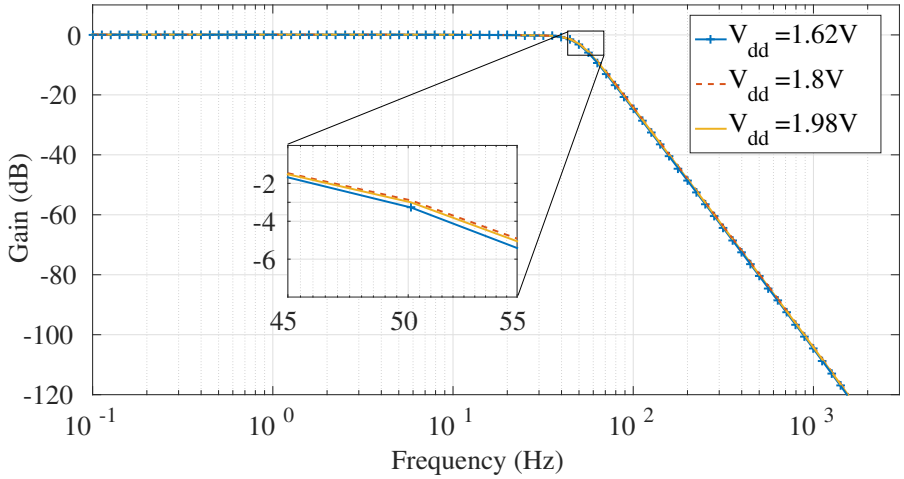


Figure 2.27: Magnitude response of the switched-g_m-C filter for 10% change in supply voltage at typical corner and room temperature.

Table 2.3: Summary of the filter performance at 1.8 V Supply.

PARAMETERS	Filter-1 (Post-layout)	Filter-2 (Post-layout)
Current consumption (μA)	0.32	0.64
Power (μW)	0.57	1.14
DC Gain (dB)	0	0
Filter Order	4	4
Bandwidth (Hz)	1 Hz–100 Hz	30 mHz–100 Hz
Linearity @1 % THD ($V_{in,pk-pk}$ (mV) @ 10 Hz)	196	180
IRN (μV_{rms}) (10 mHz–100 Hz)	109	132.6
Dynamic range (dB)	56.06	53.62

is inversely proportional to its W-L product (gate area) (Veeravalli *et al.* 2002*a*,Lee and Cheng 2009). It is to be noted that, the gate area of the transistors in the proposed filter have been kept sufficiently large for the reasons outlined in Section 2.3.1, which

in turn helps in keeping the flicker noise to a sufficiently low value.

The requirement on inband input referred noise of the filter for a given input voltage and SNR is given by (Lee and Cheng 2009)

$$Noise_{in,ref}(rms) \leq \frac{V_{in,rms}}{10^{SNR(dB)/20}} \tag{2.46}$$

In Lee and Cheng (2009), it is also stated that for filtering biomedical signals like ECG, the SNR requirement of the filter depends on maximum and minimum ECG levels and has been shown that the SNR requirement on the filter is ≥ 38 dB. Similarly, for EEG the requirement on SNR is 40 dB (Bronzino 2006). The proposed filters offer Dynamic Range in excess of 50 dB. This clearly shows that the noise contributed by proposed filters is well within the range to cause any significant performance degradation.

Note that Filter-1 and Filter-2 can process input voltage upto $196\,\mathrm{mV}_{pp}$ and $180\,\mathrm{mV}_{pp}$ respectively. For SNR > 40 dB, the input referred noise of these filters must be less than $692.96\,\mu\mathrm{V}_{rms}$ and $664.68\,\mu\mathrm{V}_{rms}$ respectively as per equation (2.46). Therefore, the proposed filters offering input referred noise of $109\,\mu\mathrm{V}_{rms}$ and $132.6\,\mu\mathrm{V}_{rms}$ (respectively) can definitely be good candidates for processing biomedical signals.

Table 2.4 compares the simulation results of proposed filters to other low-frequency filters reported in the literature. For conciseness, only low frequency filters with order four and above are included in this table. Both proposed filters exhibit comparable linearity, dynamic range and Figure-of-Merit (FoM), when compared to most recent papers in the literature.

Table 2.4: Comparison of the circuit performance with related works.

Parameters	Lo and Hung (2007)	Lee and Cheng (2009)	Liu *et al.* (2012)	Mahmoud *et al.* (2013)	Arya and Oliveira (2016)	Sun and Lee (2018)	This Work Filter-1	This Work Filter-2
V_{DD} (V)	1.8	1.5	3	±0.8	0.9	1	1.8	1.8
Technology (μm)	0.18	0.18	0.35	0.25	0.13	0.18	0.18	0.18
Power (μW)	200	0.453	0.75	30	2.8	0.35	0.57	1.14
DC Gain (dB)	-6	-9.5	-6	-5	5.9	-8	0	0
Filter Order	5	5	4	5	4	5	4	4
Bandwidth (Hz)	250	250	40	243	52	50	50	50
THD (dB)	-44	-48.6	-59	-40	-40	-49.9	-40	-40
Dynamic range (dB)	52	50	54	65	43.22	49.8	56.06	53.62
IRN (μV_{rms})	266	340	500	36	24.4	97	109	132.6
FoM †($\times 10^{-9}$)	100	0.286	0.374	3.3	4.83	0.226	0.224	0.594

$$^{\dagger}\ \text{FoM (Liu } \textit{et al.}\ (2012)) = \frac{\text{Power}}{\text{Order} \times \text{Dynamic range}}$$

Chapter 3

DESIGN OF LOW FREQUENCY SUB-THRESHOLD SOURCE FOLLOWER LOW PASS FILTER

3.1 Introduction

In wearable and implantable bio-medical devices, the major design concerns are minimizing the power consumption and noise contribution by active devices. One possible solution is to design the circuits with fewer number of active devices. In low frequency filter topologies, the recent trend is to use single branch filters. Source follower's are widely used to implement the single branch filters (Zhang *et al.* 2013, Sawigun and Pawarangkoon 2015, Sawigun and Thanapitak 2018*a*,*b*). The single branch filters need single branch of bias current for operation, hence they are more power-efficient when compared to the transconductor-capacitor filters. Also, these circuits offer low noise, low circuit area and low circuit complexity due to fewer number of transistors. Source follower based filters offer good linearity due to local feedback.

In this chapter, an ultra low power filter based on source follower architecture is proposed for biomedical applications. The filter cut-off frequency is made tunable by switching technique.

A basic source follower circuit is shown in Figure 3.1. It consists of two transistors M_1 and M_2, where M_1 acts a input transistor and M_2 as current source for biasing M_1. With a capacitor C at the output, this circuit can be viewed as a first order filter, the transfer function of which is given by (3.1).

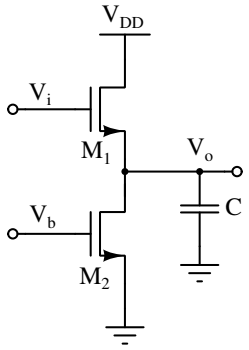


Figure 3.1: Basic source follower, with an output capacitor

$$H(s) = \frac{g_m r_{o,eq}}{sCr_{o,eq} + (g_m + g_{mb})r_{o,eq} + 1} \tag{3.1}$$

where g_m and g_{mb} are the gate transconductance and back-gate transconductance of the transistor M_1 respectively, $r_{o,eq}\,(= r_{o1}||r_{o2})$ is the equivalent output resistance.

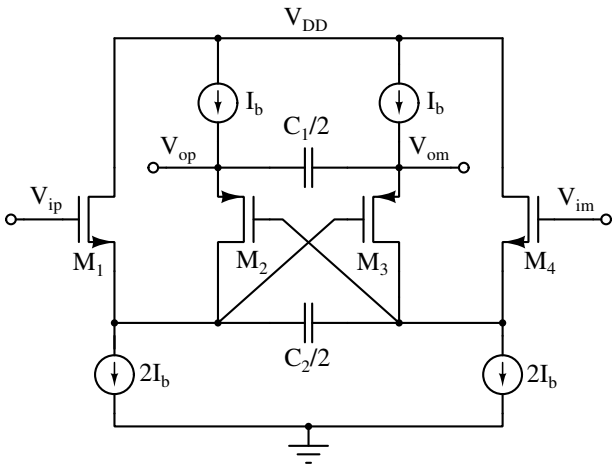
The source follower circuit can be easily extended to build a biquadratic cell to offer a second order low pass response. When designing for biomedical application the filter bandwidth is expected to be small, less than 100 Hz. The large time constant required for achieving low bandwidth with the use of on-chip capacitances, transistors are usually operated in the sub-threshold region.

3.2 Sub-threshold Source Follower (SSF) Based Bi-quadratic Cell

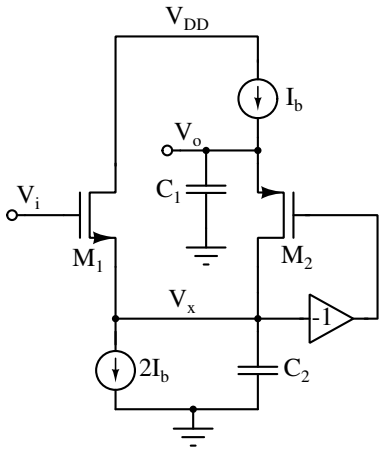
The source follower shown in Figure 3.1 is extended to realize a bi-quadratic cell as shown in Figure 3.2a. The circuit elements include four transistors ($M_1 - M_4$), four current sources (of value $I_b, 2I_b$) and two floating capacitors ($C_1/2, C_2/2$). Here, a positive feedback generated by transistors (M_2, M_3) is utilized to generate a pair of complex conjugate poles required for the second order response. Source follower based biquad's are reported in D'Amico *et al.* (2006). However, the architecture shown in Figure 3.2a has not been found to be explored further for low power, low frequency filter applications.

Source follower based biquad's exhibit the following advantages: Additional common mode feedback circuit is not required as the output common mode voltage is

self-biased by the transistor's V_{GS}, saving area and power. The circuit is free from the effects of parasitics as there are only two pairs of nodes are present, each pair forming an integrating node. Further, there are no instability issues because of positive feedback as the loop gain is inherently less than one. Also, it exhibits a low output impedance to drive the later stages and offers excellent linearity, as the signal is processed in terms of voltage by local feedback. The equivalent half circuit of Figure 3.2a



(a)



(b)

Figure 3.2: (a). Source follower biquad (b). It's equivalent half-circuit.

is shown in Figure 3.2b. It's small signal equivalent circuit is shown in Figure 3.3. The complete transfer function of the biquad is derived below. Applying Kirchhoff's

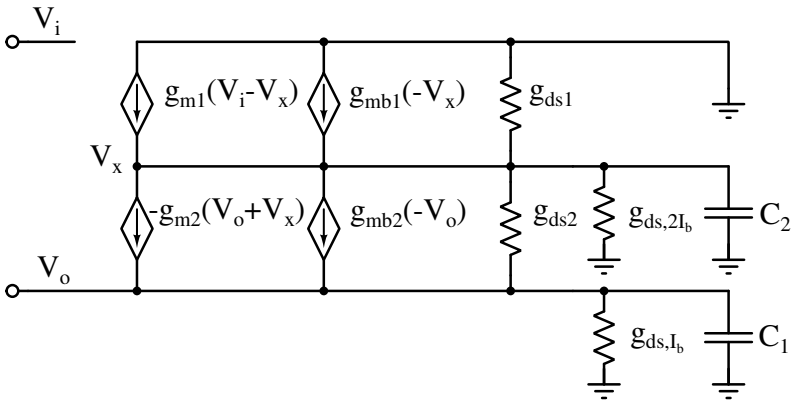


Figure 3.3: Small signal equivalent.

current law (KCL) at node V_x, one can write

$$\begin{aligned} g_{m1}V_i - (g_{m1} + g_{mb1} + g_{ds1} + g_{ds3} + sC_2)V_x \\ +g_{m2}(V_o + V_x) + g_{mb2}V_o + g_{ds2}(V_o - V_x) \quad = \quad 0 \end{aligned} \tag{3.2}$$

Similarly applying KCL at node V_o, one can write,

$$-(g_{m2} + g_{mb2} + g_{ds2} + g_{ds4} + sC_2)V_o - V_x(g_{m2} - g_{ds2}) = 0 \tag{3.3}$$

Substituting for V_x in (3.2) from (3.3), the transfer function can be written as,

$$\begin{aligned} \frac{V_o}{V_i} = -\frac{g_{m1}(g_{m2} - g_{ds2})}{(g_{mn1} - g_{m2} + g_{ds1} + g_{ds2} + g_{ds,2I_b} + sC_2)(g_{mp2} + g_{ds2} + g_{ds,I_b} + sC_1)} \\ +(g_{mp2} + g_{ds2})(g_{m2} - g_{ds2}) \end{aligned} \tag{3.4}$$

where $g_{mn1} = g_{m1} + g_{mb1}$ and $g_{mp2} = g_{m2} + g_{mb2}$. The transfer function in (3.4) represent a second order low pass filter.

If channel-length modulation is neglected, (3.4) can be simplified to a form given in (3.5)

$$\frac{V_o}{V_i} = -\frac{A_o}{\left(\frac{s}{\omega_p}\right)^2 + \frac{1}{Q}\frac{s}{\omega_p} + 1} \tag{3.5}$$

where, A_o, ω_p and Q are given by (3.6), (3.7) and (3.8) respectively.

$$A_o = \frac{1}{\left(1 + \frac{g_{mb1}}{g_{m1}}\right)\left(1 + \frac{g_{mb2}}{g_{m2}}\right)} \tag{3.6}$$

$$\omega_p = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{3.7}$$

$$Q = \frac{g_{mn1}g_{mp2}}{C_2g_{mp2} + C_1(g_{mn1} - g_{m2})}\sqrt{\frac{C_1C_2}{g_{m1}g_{m2}}} \tag{3.8}$$

A_o is the DC gain (passband gain) of the filter, ω_p is the pole frequency and Q is the quality factor. It can be seen that the DC gain A_o depends on the raio of g_{mb}/g_m of transistors M_1 and M_2. This ratio is typically in between $0.2 - 0.5$ and therefore, one cannot expect unity passband from this filter. The passband gain achievable is in the range $-3.2\,\text{dB}$ to $-7.2\,\text{dB}$.

3.3 Switched SSF Biquad Based Second Order Low Pass Filter

To enhance the re-usability of the filter and to extract wide frequency bio-potential signals, the filter cut-off should be tunable. The filter cut-off is made tunable by adopting a switching strategy, like the one adopted in chapter 2. However, the architecture being entirely different from that in chapter 2, a different has been adopted for switching. The filter is switched by switching the bias current of the transistors with a required duty-ratio (D).

The effect is that the transconductance of g_{mn1} and g_{mp2} of transistors M_1 and M_2 scale with D (Note g_m is directly proportional to the drain current I_D in sub-threshold region of operation). Since, the capacitors remain constant, the pole frequency and hence the bandwidth scales proportionally with D. It is to be noted that the Q of the filter is not affected by D, as evident from (3.8).

The schematic of the proposed switched second order LPF based on the source

follower biquad cell is shown in Figure 3.4. A reference current I_{ref} is mirrored using transistors M_{12} and M_{13}. The current flowing out of M_{13} is switched using the switch S_1, generating a pulsed current I_{pulse} which is mirrored to SSF biquad cell.

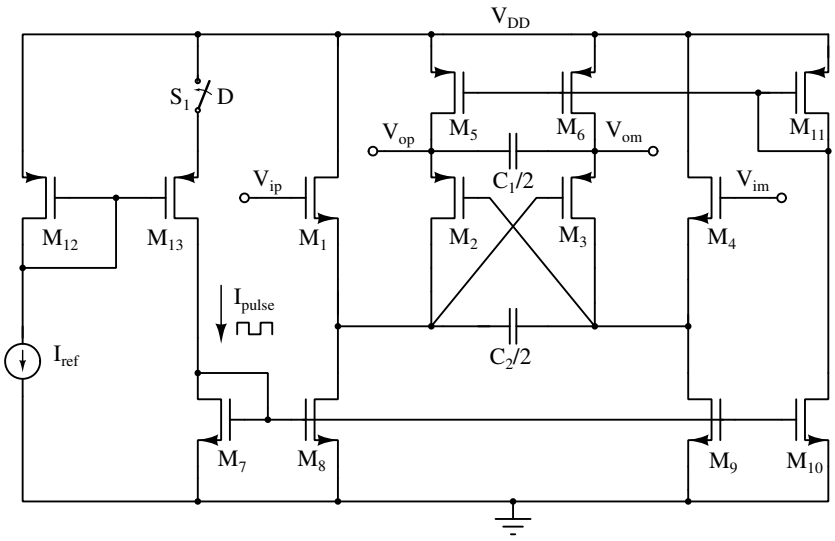


Figure 3.4: Schematic of switched second order LPF

In weak-inversion region, the transconductance of transistor is $g_m = I_D/\eta V_T$. The thermal voltage V_T is proportional to the absolute temperature (PTAT) and therefore, g_m (and the cut-off frequency) decreases with the temperature. g_m and hence the bandwidth can be made compensated for temperature, if the drain current I_D is made PTAT. This calls for a PTAT current reference generation circuit.

3.3.1 Switched PTAT Current Reference

In this section, a circuit for generating and switching bias current is presented.

3.3.1.1 Classical Beta Multiplier Current Reference Circuit

A classical beta multiplier current reference circuit is shown in Figure 3.5 (Vittoz and Fellrath 1977). The circuit consists of four transistors M_1-M_4 and one resistor R. The sizes of transistors M_1, M_3 and M_4 are identical and M_2 is p times larger. p is the mirroring ratio (usually in the range $2-4$). The transistors M_3 and M_4 keeps the current equal, on both the sides.

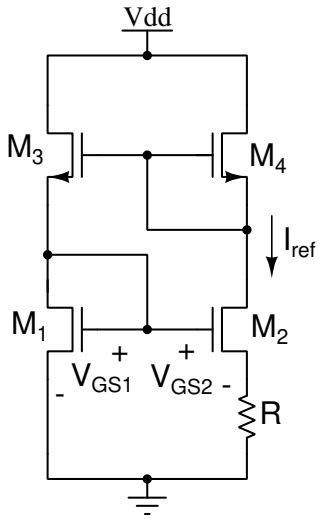


Figure 3.5: Classical beta multiplier current reference.

By applying KVL, we can write

$$V_{GS1} = V_{GS2} + I_{ref}R \tag{3.9}$$

The reference current I_{ref} is expressed as

$$I_{ref} = \frac{V_{GS1} - V_{GS2}}{R} \tag{3.10}$$

Assuming all transistors are operating in sub threshold region,

$$V_{GS1,2} = \eta V_T ln\left(\frac{I_{D1,2}}{I_{Do} \cdot K_{1,2}}\right) + V_{TH1,2} \tag{3.11}$$

where $K = W/L$ is the aspect ratio of transistor, $I_{Do} = \mu C_{ox}(\eta - 1)V_T^2$ is the pre-exponential factor of sub-threshold current, μ is the carrier mobility, C_{ox} is the gate-oxide capacitance and V_{TH} is the threshold voltage. The expression for I_{ref} can be expressed as

$$I_{ref} = \frac{\eta V_T ln(p)}{R} = \frac{\eta kT ln(p)}{qR} \tag{3.12}$$

where $p = K_2/K_1 = (W/L)_2/(W/L)_1$ is the ratio of transistor sizes, k is the Boltzmann constant, T is the absolute temperature and q is the electron charge.

3.3.1.2 Modified Current Reference Circuit with Switching

The classical beta multiplier circuit has been modified suitably with cascode transistors and associated switching circuitry to generate a switched PTAT current reference required for the purpose. The complete current reference circuit is shown in Figure 3.6.

The sub-threshold current I_D through a PMOS transistor is given by,

$$I_D = KI_{Do}\, exp\left(\frac{V_{SG} - |V_{TH}|}{\eta V_T}\right)\left(1 - exp\left(\frac{-V_{SD}}{\eta V_T}\right)\right) \tag{3.13}$$

For V_{SD}>4V_T, (3.13) reduces to

$$I_D = KI_{Do}\, exp\left(\frac{V_{SG} - |V_{TH}|}{\eta V_T}\right) \tag{3.14}$$

The reference current I_{ref} in Figure 3.6 is expressed as

$$I_{ref} = \frac{V_{SG7} - V_{SG8}}{R} \tag{3.15}$$

Substituting for V_{SG7} and V_{SG8} from (3.14) and by considering same drain currents, I_{ref} is given by

$$I_{ref} = \frac{\eta V_T ln(p)}{R} = \frac{\eta kT ln(p)}{qR} \tag{3.16}$$

where $p = K_8/K_7 = (W/L)_8/(W/L)_7$ is the ratio of transistor sizes. With a thermally stable external resistor, the I_{ref} is found to be PTAT. In this work, $R = 10\,\mathrm{M\Omega}$ is chosen to generate a nano-ampere current reference ($I_{ref} = 1.47\,\mathrm{nA}$). From (3.16), it is also evident that the reference current varies proportional to the absolute temperature (PTAT) and it is clearly shown in the Figure 3.7.

For the current reference circuit designed in this work, I_{ref} is plotted as a function of V_{DD} at room temperature in Figure 3.8. A line sensitivity of 0.9%/V is observed in a supply range of 0.8 to 1.8 V, proving that the reference current is almost independent of supply voltage. The generated current reference is mirrored and switched using the transistors $M_9 - M_{14}$ as shown in Figure 3.6. Here, the duty ratio of V_{pulse} is varied to switch the bias currents of the transconductors. A complete schematic of the proposed switched SSF biquad based second order LPF is as shown in Figure 3.9. Regulated cascode current mirror has been used for accurate mirroring of the switched current. The transistor sizes for the proposed filter are listed in Table 3.1.

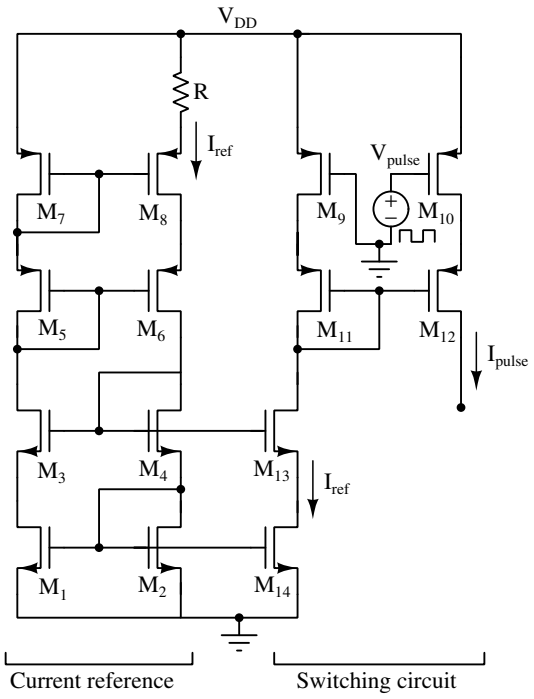


Figure 3.6: Current reference generator circuit with switching.

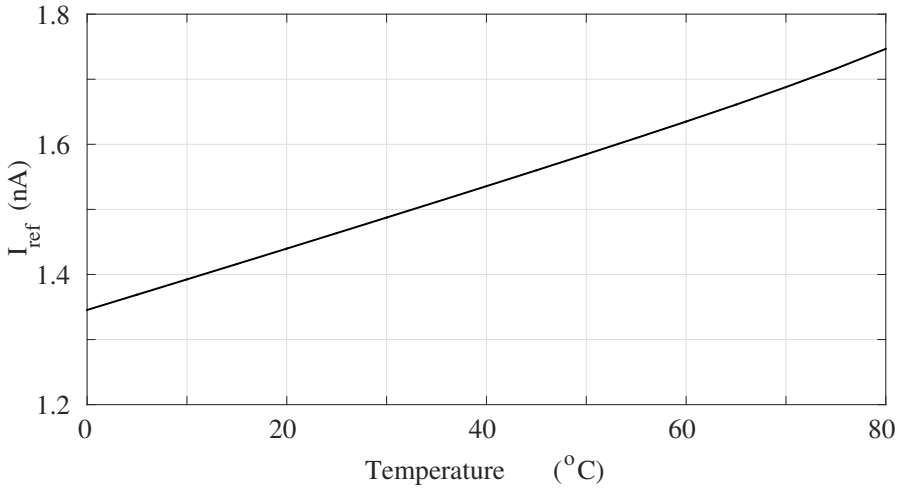


Figure 3.7: I_{ref} as a function of temperature.

3.3.2 Noise Analysis

The noise model of SSF biquad is shown in Figure 3.10. In transistors, the major noise sources are flicker noise and thermal noise. For noise analysis, both flicker noise and

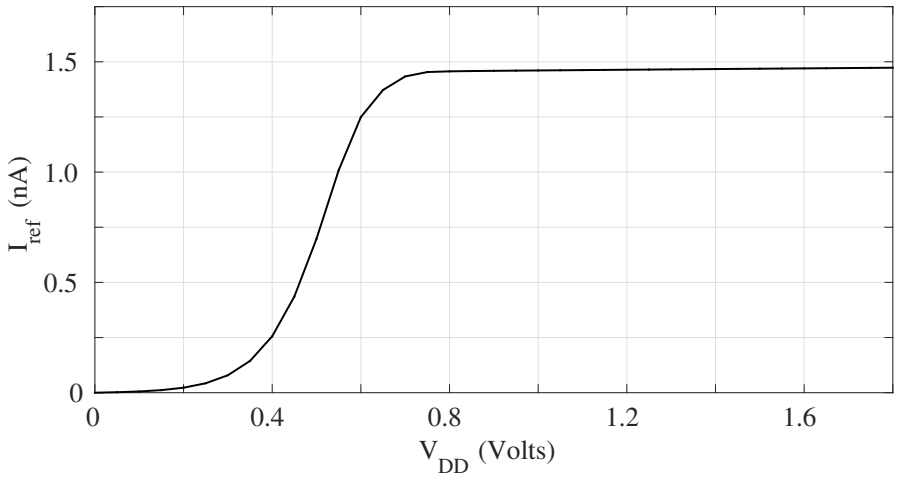


Figure 3.8: I_{ref} as a function of V_{DD} at room temperature.

Table 3.1: Transistor sizes of the proposed filter

Transistor	$W(\mu m)/L(\mu m)$
$M_{1-4,13,14}$	2 (2/1)
$M_{5,7}$	2 (6/1)
$M_{6,8}$	2 (9/1)
M_{9-12}	2 (1/0.5)
M_{15}	4 (12/18)
M_{16}	6 (16/10)
M_{17}	6 (16/18)
M_{18-20}	2 (1/10)
$M_{21,22,24,25}$	4 (12/18)
M_{23}	4 (6/18)
M_{26-30}	6 (16/12)

thermal noise are considered.

The noise currents $I_{n1,th}$ and $I_{n2,th}$ are due to thermal noise. Noise voltages $V_{n1,f}$ and $V_{n2,f}$ are due to flicker noise. $V_{n,out}$ is the output noise voltage. The total output

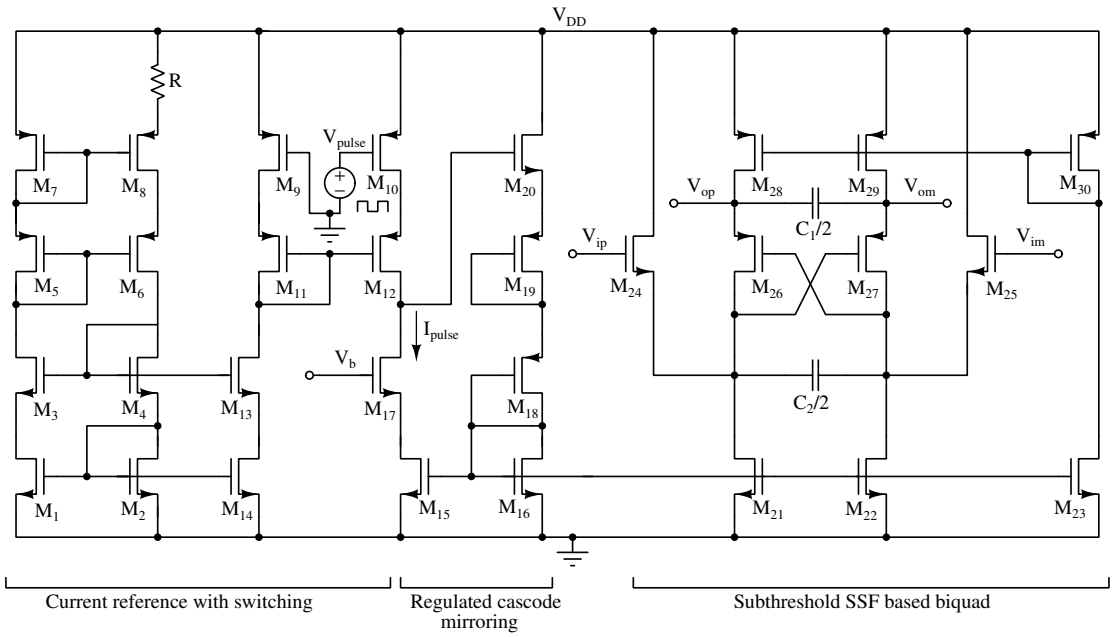


Figure 3.9: Complete schematic of the switched SSF biquad based second order low pass filter.

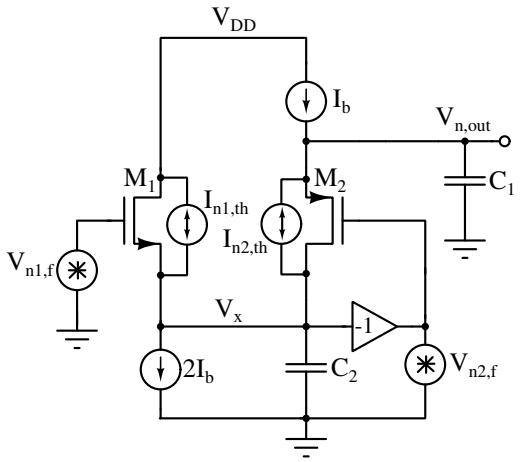


Figure 3.10: Equivalent noise model of SSF biquad for analysis.

thermal noise is,

$$\overline{V_{n,out,th}^2} = \overline{V_{n1,out,th}^2} + \overline{V_{n2,out,th}^2} \tag{3.17}$$

where $\overline{V_{n1,out,th}^2}$ and $\overline{V_{n1,out,th}^2}$ are the output thermal noise voltages due to noise currents $I_{n1,th}$ and $I_{n2,th}$ respectively. The output thermal noise voltage $\overline{V_{n1,out,th}^2}$ is

expressed as follows,

$$V_{n1,out,th} = \frac{g_{m2}}{g_{m2}+g_{mb2}} \cdot \frac{I_{n1,th}}{g_{m1}} \cdot \frac{g_{m1}}{g_{m1}+g_{mb1}}$$

$$\overline{V^2_{n1,out,th}} = \frac{\overline{I^2_{n1,th}}}{(g_{m1}+g_{mb1})^2} \cdot \left(\frac{g_{m2}}{g_{m2}+g_{mb2}}\right)^2 \tag{3.18}$$

For simplicity, we have neglected the channel length modulation. The output thermal noise voltage $\overline{V^2_{n2,out,th}}$ is,

$$V_{n2,out,th} = \frac{g_{m2}}{g_{m2}+g_{mb2}} \cdot \frac{I_{n2,th}}{g_{m2}}$$

$$\overline{V^2_{n2,out,th}} = \frac{\overline{I^2_{n2,th}}}{(g_{m2}+g_{mb2})^2} \tag{3.19}$$

By substituting (3.18) and (3.19) in (3.22), the total output thermal noise is given by

$$\overline{V^2_{n,out,th}} = \frac{\overline{I^2_{n1,th}}}{(g_{mn1})^2} \cdot \left(\frac{g_{m2}}{g_{mp2}}\right)^2 + \frac{\overline{I^2_{n2,th}}}{(g_{mp2})^2} \tag{3.20}$$

Thus, the total input referred thermal noise voltage, for the filter DC gain A_o defined in (3.6) can be written as

$$\overline{V^2_{n,in}} = \frac{4kT\gamma}{g_{m1}}\left[1 + \frac{g^2_{mn1}}{g_{m1}g_{m2}}\right] \tag{3.21}$$

Similarly, the total output flicker noise can be written as,

$$\overline{V^2_{n,out,f}} = \overline{V^2_{n1,out,f}} + \overline{V^2_{n2,out,f}} \tag{3.22}$$

The flicker noise voltage due to transistor M_1 is

$$V_{n1,out,f} = V_{n1,f}\left[\frac{g_{m1}g_{m2}}{g_{mn1}g_{mp2}}\right] \tag{3.23}$$

and flicker noise voltage due to M_2 is given by

$$V_{n2,out,f} = V_{n2,f}\left[\frac{g_{m2}}{g_{mp2}}\right] \tag{3.24}$$

The total output flicker noise voltage is given by

$$\overline{V_{n,out,f}^2} = \frac{K_F}{(WL)_1 C_{ox} f}\left[\frac{g_{m1}g_{m2}}{g_{mn1}g_{mp2}}\right]^2 + \frac{K_f}{(WL)_2 C_{ox} f}\left[\frac{g_{m2}}{g_{mp2}}\right]^2 \tag{3.25}$$

Thus, the total input referred flicker noise voltage is:

$$\overline{V_{n,in,f}^2} = \frac{K_F}{C_{ox}\cdot f}\left[\frac{1}{(WL)_1}\right] + \frac{g_{mn1}^2}{(WL)_2 \cdot g_{m1}^2} \tag{3.26}$$

The overall input-referred-noise (IRN) of the biquad due to both thermal and flicker noise is given by

$$\overline{V_{n,in}^2} = \overline{V_{n,in,th}^2} + \overline{V_{n,in,f}^2} \tag{3.27}$$

$$\begin{aligned}\overline{V_{n,in}^2} = \frac{4kT\gamma}{g_{m1}}\left[1 + \frac{g_{mn1}^2}{g_{m1}g_{m2}}\right] \\ + \frac{K_F}{C_{ox}\cdot f}\left[\frac{1}{(WL)_1} + \frac{g_{mn1}^2}{(WL)_2 \cdot g_{m1}^2}\right]\end{aligned} \tag{3.28}$$

The input-referred-noise (IRN) of the biquad integrated over the passband is given by

$$\overline{V_{n,in}^2} = \left(\overline{V_{n,in,th}^2} + \overline{V_{n,in,f}^2}\right)\cdot \Delta f \tag{3.29}$$

$$\begin{aligned}\overline{V_{n,in}^2} = \frac{4kT\gamma}{g_{m1}}\left[1 + \frac{g_{mn1}^2}{g_{m1}g_{m2}}\right]\cdot \Delta f \\ + \frac{K_F}{C_{ox}\cdot f}\left[\frac{1}{(WL)_1} + \frac{g_{mn1}^2}{(WL)_2 \cdot g_{m1}^2}\right]\cdot \Delta f\end{aligned} \tag{3.30}$$

where, γ is the noise co-efficient, K_F is the flicker noise coefficient, f is the frequency. Flicker noise, being inversely proportional to the transistor gate area, can be reduced by choosing a large sized transistors so as to make the thermal noise the dominant contributor. The thermal noise integrated over the passband is given by

$$\overline{V_{n,in}^2} = \frac{4kT\gamma}{\sqrt{C_1 C_2}}\sqrt{\frac{g_{m2}}{g_{m1}}}\left[1 + \frac{g_{mn1}^2}{g_{m1}g_{m2}}\right] \tag{3.31}$$

Assuming all transistors have same gate transconductanes and by neglecting body-

effect, the thermal noise is equal to

$$\overline{V_{n,in}^2} = \frac{8kT\gamma}{\sqrt{C_1 C_2}} \tag{3.32}$$

From (3.32), it is evident that thermal noise reduces with higher load capacitors. In the proposed filter, with the value of capacitors used, the noise offered is made sufficiently low.

3.4 Simulation Results

A second order Butterworth LPF is designed using the proposed switched SSF biquad in UMC 0.18 μm CMOS technology. The filter is designed to operate in the weak inversion region with a supply voltage of 1.8 V. The complete layout of the filter is shown in Figure 3.11. The layout area is 0.121 mm^2. Post layout simulations are carried out to evaluate the filter performance. The summary of the filter performance is shown in Table 3.2.

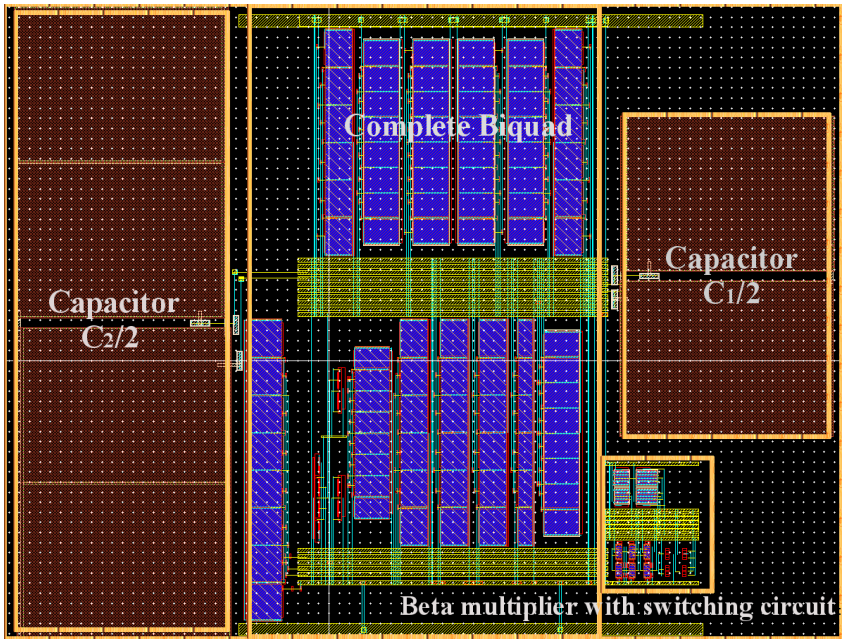


Figure 3.11: Complete layout of the switched SSF biquad filter (Area=0.121 mm^2).

The magnitude response of the filter for various duty ratio (D) settings of the current pulse is shown in Figure 3.12. The filter cut-off frequency f_c is tunable from

Table 3.2: Summary of the filter performance at 1.8 V supply.

PARAMETERS	Values
Current consumption (nA)	14.42
Power (nW)	25.95
DC gain (dB)	-3.25
Filter order	2
Bandwidth (Hz)	4–100
Linearity @1 % THD	996
($V_{in,pk-pk}$ (mV) @ 10 Hz)	
IRN (μV_{rms})	8.985
(100 mHz–100 Hz)	
Dynamic range (dB)	91.86

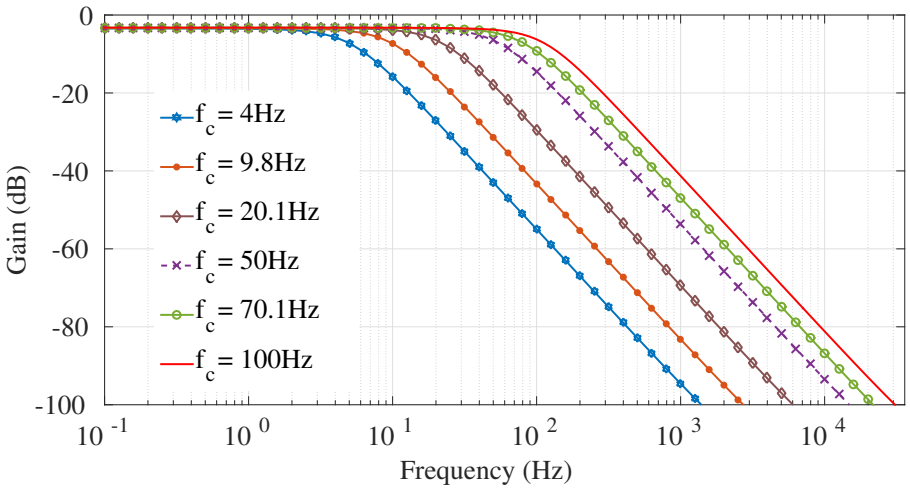


Figure 3.12: Magnitude response of the filter with duty ratio tuning. The tuning range is from 4 Hz to 100 Hz. The following settings are used for the results and in the format [clock frequency, duty cycle, cut-off frequency]: [1 kHz, 1%, 4 Hz], [10 kHz, 10%, 9.8 Hz], [10 kHz, 20%, 20.1 Hz], [20 kHz, 50%, 50 Hz], [20 kHz, 70%, 70.1 Hz], [20 kHz, 100%, 100 Hz] .

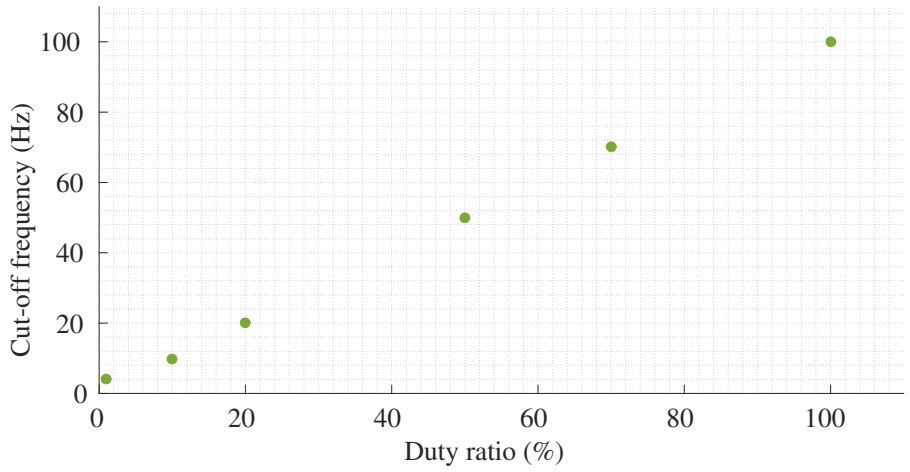


Figure 3.13: Tuning graph showing f_c for different values of duty ratio.

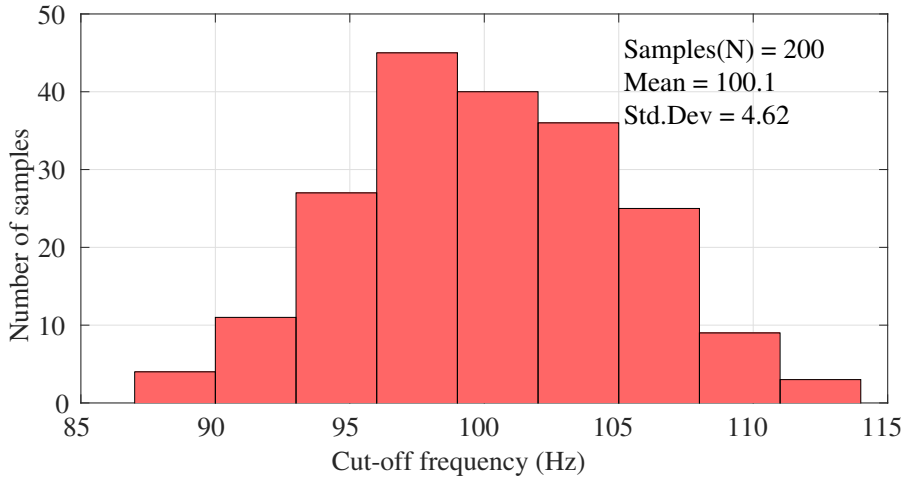


Figure 3.14: Monte-carlo simulation of the filter with 200 runs for $f_c = 100\,\text{Hz}$ setting.

4 Hz – 100 Hz for 1% to 100% duty ratio of the current pulse. Note that, the clock frequency is modified suitably to keep clock feed-through out of stop-band frequency (corresponding to attenuation of 100 dB). The integrating capacitors for the filter are $C_1/2 = 15.25\,pF$ and $C_2/2 = 30.50\,pF$ including parasitics, for the transconductance of 27.23 nS ($g_m \simeq g_{m1} \simeq g_{m2}$) to achieve bandwidth of 100 Hz with 100% duty ratio. Figure 3.13 shows the cut-off frequency of the filter as a function of duty ratio. It is evident that the cut-off frequency varies linearly with duty ratio except towards

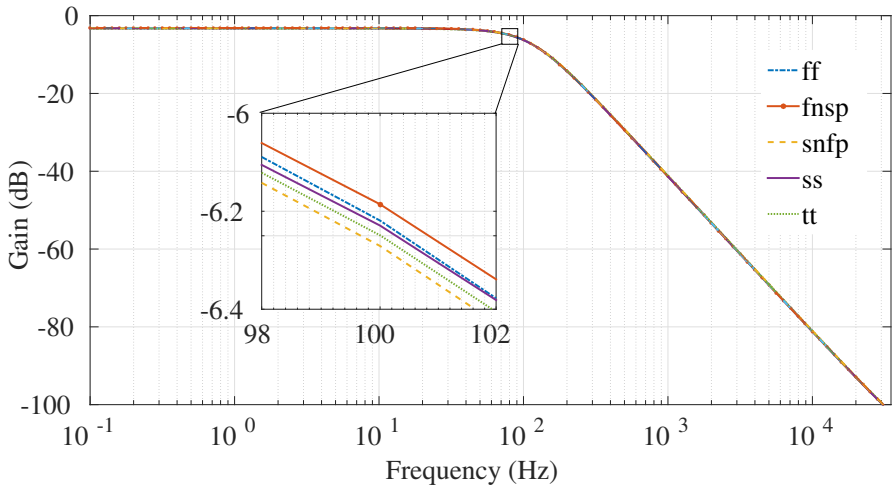


Figure 3.15: Magnitude response of the filter across process corner variations.

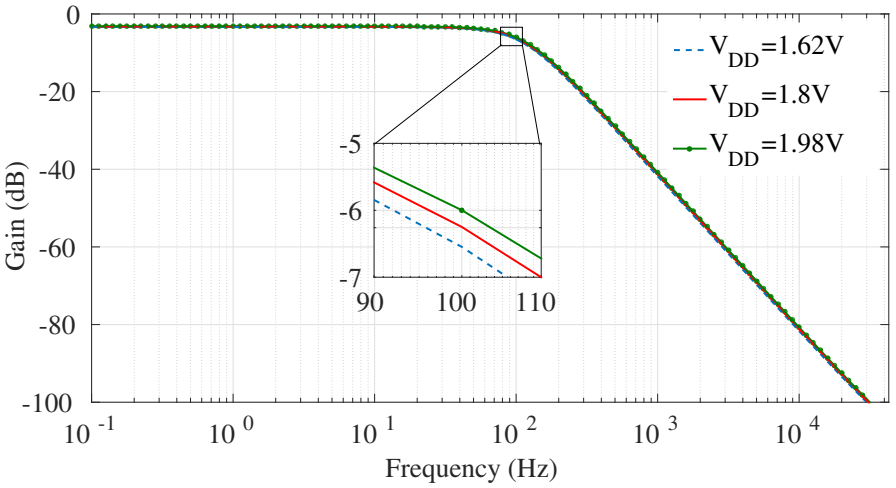


Figure 3.16: Magnitude response of the filter for variations in supply voltage.

4 Hz. Clock feedthrough charge on capacitor starts dominating over that from the switched transconductor (due to low on-time) and capacitor charge/discharge due to junction leakage (due to large off time). Monte-Carlo simulation has been carried out on the layout extracted filter to evaluate the performance in presence of transistor mismatches. The filter is set for 100 Hz bandwidth with D=100%. Figure 3.14 shows the distribution of filter cut-off frequency for 200 samples. A mean of 100.1 Hz and standard deviation (σ) of 4.62 Hz is obtained.

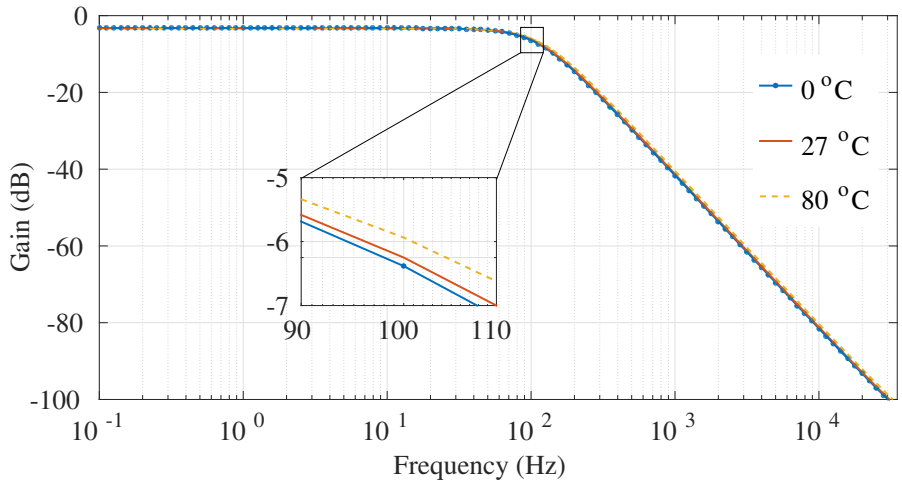


Figure 3.17: Magnitude response of the filter for change in temperature.

Post layout simulations are carried out across PVT variations, for a setting of f_c=100 Hz. Figure 3.15 shows the frequency response of the filter at various process corners. The change in cut-off frequency f_c is less than 1% at nominal supply voltage of 1.8 V and at room temperature (27°C). The magnitude response for ±10% variation in supply voltage from the nominal value at typical process corner and room temperature is as shown in Figure 3.16. The change in bandwidth is less than 5%. For a temperature in the range 0°C to 80°C at nominal supply voltage and typical corner, the bandwidth variation is less than 5% as shown in Figure 3.17.

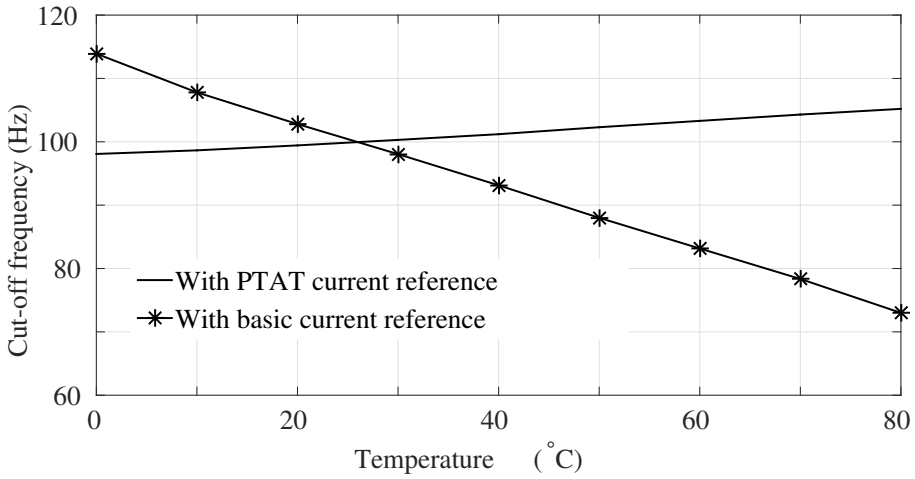


Figure 3.18: Cut-off frequency (f_c) vs temperature (T).

It is to be noted that, the robustness of bandwidth against temperature is due to the PTAT current reference circuit. To ascertain this, the cut-off frequency of the filter is plotted against the temperature for PTAT current (generated from the reference circuit) and a constant current in Figure 3.18. It can be clearly seen that the filter exhibits a poor bandwidth performance with temperature when a constant current reference is used.

The output referred noise of the filter with D=100% (100 Hz bandwidth) is shown in the Figure 3.19. The rms value of the voltage noise integrated over the band 100 mHz - 100 Hz is found to be 9.98 μV.

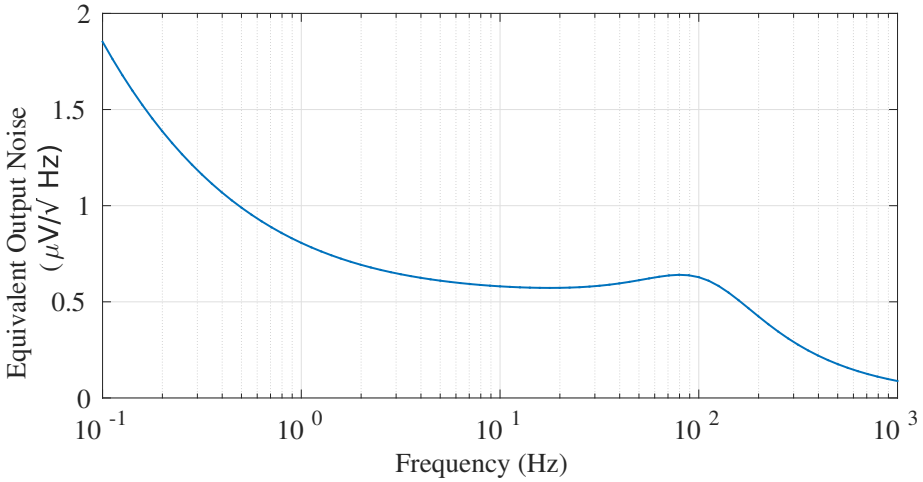


Figure 3.19: Output-referred noise of the filter.

The overall noise contributed by the filter is well within the permissible range. For biomedical applications, the acceptable in-band input referred noise of the filter is given by (2.46) With the dynamic range offered in excess of 90 dB, the overall noise contributed by proposed filter is well within the acceptable range to cause any notable performance degradation. The proposed filter can process input voltage upto 996 mV_{pp}. As per (2.46), for SNR > 40 dB the in-band input referred noise of the filter must be less than 3.52 $\mu\mathrm{V}_{rms}$. Therefore, the proposed filter offering input referred noise of 8.985 $\mu\mathrm{V}_{rms}$ is indeed the best candidate for filtering bio-signals.

The linearity performance of the filter is evaluated by single tone test, for an input voltage of 996 mV_{pp} at 10 Hz. Figure 3.20 shows output voltage spectrum of the filter. Even order harmonics are canceled out due to fully differential architecture of

the filter. Third harmonic component is the dominant contributor and third harmonic distortion (HD3) is found to be -40.05 dB. HD3 is associated with a 1% THD as higher order harmonics are negligible.

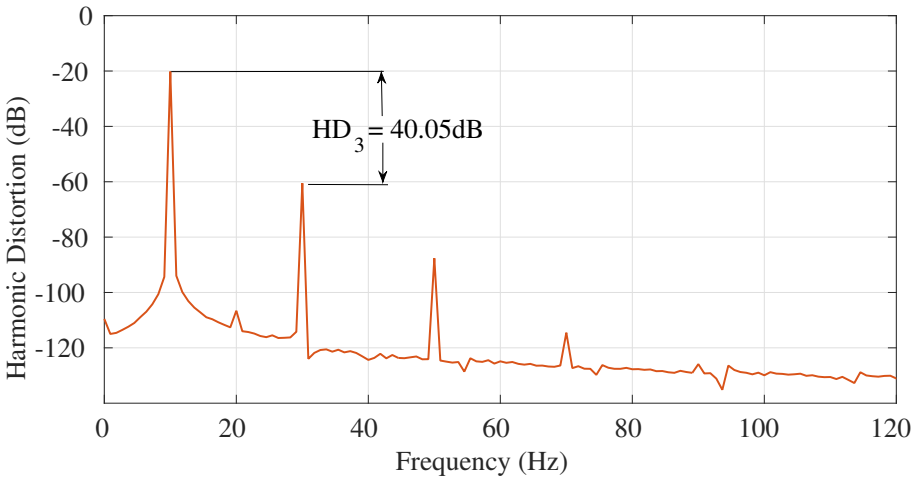


Figure 3.20: Harmonic distortion of the filter with V_{in}= $996mV_{pp}$@10Hz.

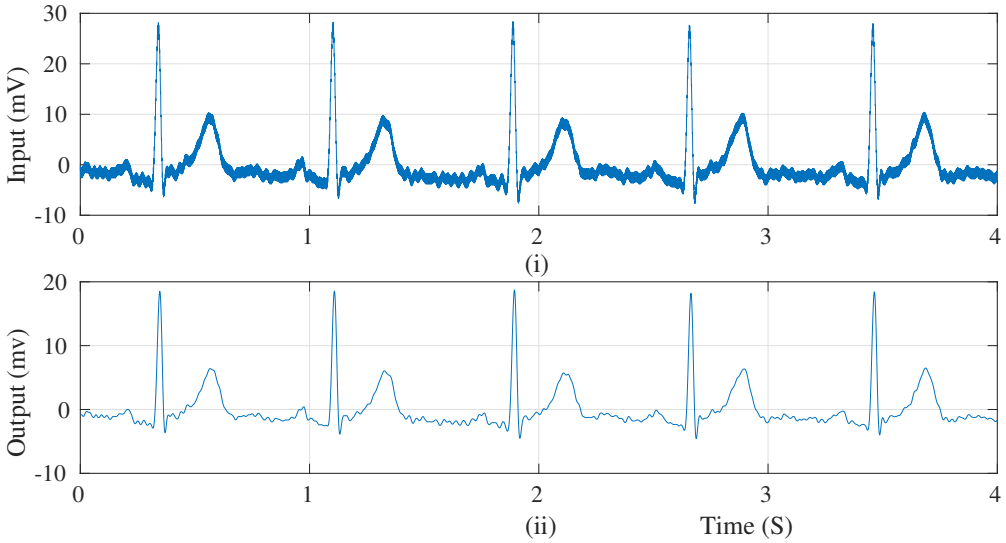


Figure 3.21: The post layout filter test for ECG:(i). The time representation of the original ECG signal (ii). The filtered ECG signal obtained from the proposed low pass filter.

The efficiency of the proposed filter is illustrated by filtering the ECG signal. The noisy ECG signal shown in the Figure 3.21(i) is generated by adding an out-of-

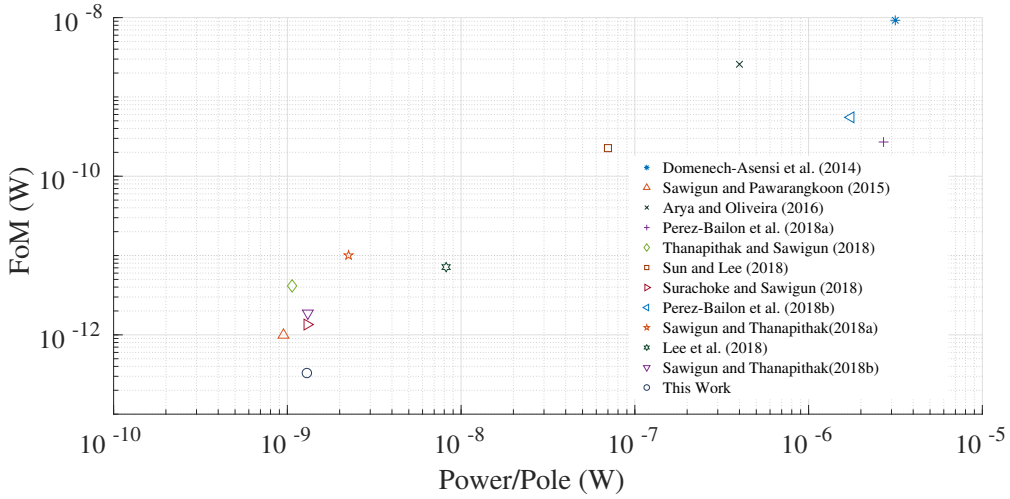


Figure 3.22: FoM vs Power/Pole.

band noise (4 mVpp, 500 Hz sinusoidal signal) to a pre-amplified original ECG signal obtained from Goldberger *et al.* (2000 (June 13). This noisy ECG signal is provided as an input to the proposed LPF with 100 Hz bandwidth. The output of the LPF is as shown in Figure 3.21(ii), and it is clearly visible that the out of band noise has been effectively filtered.

Table 3.3 compares the filter performance with the state-of-the-art filters. To validate the results, the switching duty-ratio is set to 100% with $I_b = 1.47$ nA ($f_c = 100$ Hz setting). The proposed filter being offering dynamic range (DR) as high as 91.6 dB is found to be the best when compared to other filters in the literature.

$$FoM = \frac{\text{Power}}{\text{Order} \times \text{Dynamic range}} \tag{3.33}$$

Also, it exhibits a better Figure-of-Merit (FoM) defined by Liu *et al.* (2012). Lower FoM indicates better filter performance. Figure 3.22 shows FoM plot against Power per Pole. The designed filter is best among the similar works found in the literature.

Table 3.3: Comparison of the filter performance with prior works found in the literature.

Parameters	V_{DD} (V)	Technology (μm)	Power (μW)	DC Gain (dB)	Filter Order	Bandwidth (Hz)	THD (dB)	IRN (μV_{rms})	DR (dB)	FoM
Doménech-Asensi *et al.* (2014)	3	0.35	6.31	–	2	1.95	-40	791	50.65	9.25×10^{-9}
Sawigun and Pawarangkoon (2015)	1.5	0.35	0.0019	0	2	250	-40	89	59.6	9.94×10^{-13}
Arya and Oliveira (2016)	0.9	0.13	0.8	4.1	2	47.98	-40	17.38	43.8	2.58×10^{-9}
Pérez-Bailón *et al.* (2018*a*)	1.8	0.18	2.7	0	1	5	-40	12.8	>80	2.70×10^{-10}
Thanapitak and Sawigun (2018)	0.9	0.35	0.00426	-0.05	4	100	-40	80.5	48.2	4.143×10^{-12}
Sun and Lee (2018)	1	0.18	0.35	-8	5	50	-49.9	97	49.8	2.26×10^{-10}
Surachoke and Sawigun (2018)	1.5	0.35	0.0052	0.06	4	99	-40	43.9	59.7	1.345×10^{-12}
Pérez-Bailón *et al.* (2018*b*)	1	0.18	1.75	0	1	1	-40	11.3	>70	5.533×10^{-10}
Deo *et al.* (2018)	1.8	0.18	0.689	21.8 †	3 †	200	–	81.79	–	–
Sawigun and Thanapitak (2018*a*)	0.6	0.35	0.009	-2.77	4	101	-41	46.27	47	1.005×10^{-11}
Lee *et al.* (2018)	1	0.18	0.041	-7	5	250	–	134	61.2	7.141×10^{-12}
Sawigun and Thanapitak (2018*b*)	1.5	0.35	0.00525	-0.09	4	100	-40	39.38	56.9	1.875×10^{-12}
This work	1.8	0.18	0.0259	-3.25	2	100	-40	9.985	91.86	3.3057×10^{-13}

† With pre-amplifier

Chapter 4

OUTPUT RESISTANCE ENHANCEMENT SCHEME FOR A DIFFERENTIAL AMPLIFIER

4.1 Introduction

Consider a first order filter, shown in figure 4.1. With transconductors having finite output impedance r_o, the transfer function of the filter takes the form (4.1) and cut-off frequency of the filter is decided by the ratio $\frac{g_m+g_o}{C}$ (where $g_o = 1/r_o$ and $g_{m1} = g_{m2} = g_m$).

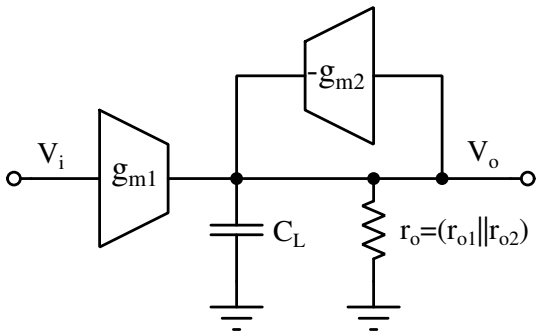


Figure 4.1: $g_m - C$ filter with transconductor having finite output impedance.

$$\frac{V_o}{V_i} = \frac{\frac{g_m}{g_m + g_o}}{1 + \frac{sC_L}{g_m + g_o}} \tag{4.1}$$

One can expect the cut-off frequency to reduce when g_m is reduced only if $g_m >> g_o$. Otherwise g_o will dominate over g_m resulting in bandwidth saturation and reduction in DC gain as it can be clearly seen from (4.1). The other alternative is to have an arrangement for scaling g_o along with g_m to keep g_m/g_o constant. The latter option has already been adopted in the designs explained in chapter 1.

In this chapter, a novel technique to enhance r_o of the transconductor is proposed. The proposed high DC gain transconductor is not only useful for realizing $g_m - C$ filters but also it can be used as OTA in applications such as sigma-delta converter, switched capacitor circuits, where precision is important.

Existing techniques such as cascoding two transistors in a stack to increase r_o, can give an enhancement in gain equal to the intrinsic gain. However, as the operating voltage scales down, cascoding limits voltage headroom. Cascading beyond two stages or other techniques such as gain boosting, requires additional compensation to stabilize the OTA in a closed loop, when used in feedback.

Cancellation of output conductance, by using a negative conductance in parallel to the output conductance can give a high r_o, without requiring additional complex compensation techniques (Yan and Geiger 2002, He *et al.* 2003). The main limitation with Yan and Geiger (2002), is the requirement of extensive tuning to maintain the enhancement over process, voltage and temperature (PVT) variations. Further, the enhancement in DC gain degrades with output voltage swing, due to the non-linearity of the elements (arising at large voltage swing) used in the arrangement to cancel the output conductance. In He *et al.* (2003), an output level monitoring circuit and digital tuning circuit is used to maintain large DC gain over output voltage swing. In Huang and Chen (2014), a conductance cancellation technique that is insensitive to PVT and output voltage swing variation has been proposed. However, the enhancement that can be obtained is in the neighborhood of intrinsic gain of the transistor.

Another limiting factor to the use of negative conductance cancellation technique is the fact that the OTA can have a dominant right half plane (RHP) pole, if the negative conductance is greater than the output conductance. In Yan (2002), the stability and meta stability of a closed loop system with an unstable open loop system has been studied. It has been shown that the dominant RHP pole can move to the left half plane (LHP) when connected in feedback, and hence the closed loop system can still be stable.

This work presents a conductance cancellation technique in which an enhancement

of about two-to-three folds of intrinsic gain (in dB) can easily be obtained due to enhancement in r_o. In other words, the enhancement is equivalent to three amplifier stages (each having gain equal to intrinsic gain) in cascade. The proposed technique, is simple in design and is relatively insensitive to PVT variations. By using an arrangement of a gyrator based linear attenuator and a transconductor to cancel the output conductance, the technique provides significant boost in DC gain across large output voltage swing.

4.2 Concept of Conductance Cancellation

An approach for canceling the effect of output resistance r_o of a transconductor is to supply a current equal to that drawn by r_o. This in turn can be achieved by supplying a current to the output node through another transconductor whose input voltage is tuned based on the current drawn by r_o. By doing this the current drawn by the r_o is made approximately zero, thus canceling the output conductance.

The proposed output conductance cancellation scheme is shown in Figure 4.2. g_m is the main transconductor whose output resistance is to be enhanced, g_{mc} is the transconductor used to enhance the output resistance and r_o is the effective resistance at the output node (accounting for the output resistance of both g_m and g_{mc}). As long as the current drawn by r_o is supplied by g_{mc}, the main transconductor g_m is free of loading from r_o and therefore, the DC gain offered by the main transconductor can be made infinite, ideally.

Input to g_{mc} is an attenuated form of the output v_o (through an attenuator block of gain α). The degree to which the output resistance of the main transconductor g_m is enhanced, is decided by the accuracy of the current provided by g_{mc} being equal to the current drawn by r_o.

The effective resistance at the output node, r_{out} of the circuit, in Figure 4.2 is given by the expression,

$$r_{out} = \frac{r_o}{1 - \alpha g_{mc} r_o} \tag{4.2}$$

From (4.2), it is evident that r_{out} of the circuit goes to infinity, as α approaches $\frac{1}{g_{mc} r_o}$. If α is very small, then the voltage swing at node v_x is very small. This implies that the output current of g_{mc} is linear. Hence, the proposed conductance cancellation

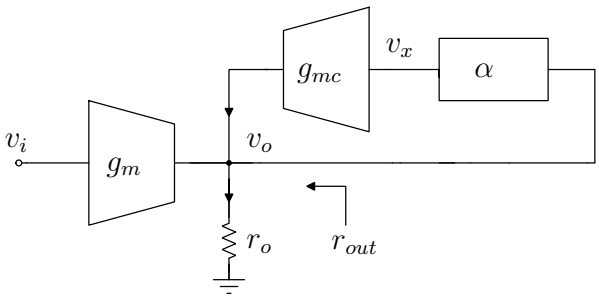


Figure 4.2: Cancellation of output conductance of a Transconductor.

method is linear. Though this concept of cancellation is similar to that proposed in He *et al.* (2003), the approach used to realize the circuit is novel and simple.

4.3 Circuit Realization

A gyrator based circuit is proposed to realize the attenuator with α close to $\frac{1}{g_{mc}r_o}$. The proposed scheme is shown in Figure 4.3. Input to the attenuator is the output v_o of the main transconductor in Figure 4.2 and the output is v_x. The attenuator consists of transconductor g_{m1} and a gyrator formed by g_{m2} and $-g_{m1}$. r_{o2} and r_{o1} are output resistances of g_{m2} and g_{m1} respectively.

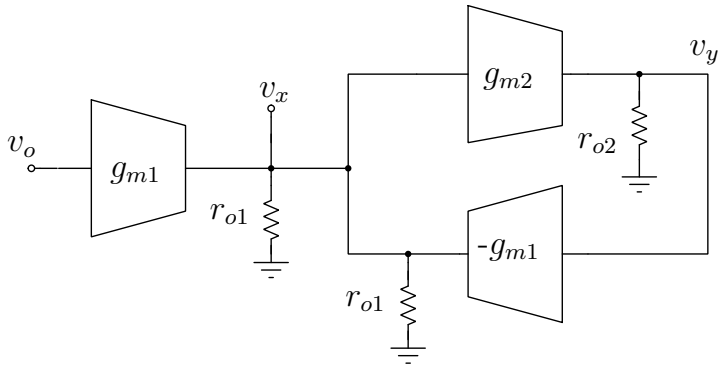


Figure 4.3: Realization of the attenuator block α

For the ease of analysis, Figure 4.3 is redrawn in Figure 4.4. Here the attenuator is viewed as comprising input transconductor, forward transresistance amplifier with a

gain of $R_{ol} = \frac{g_{m2}r_{o2}r_{o1}}{2}$, and a feedback transconductor of transconductance $G_f = g_{m1}$. The effective impedance at node v_x will be,

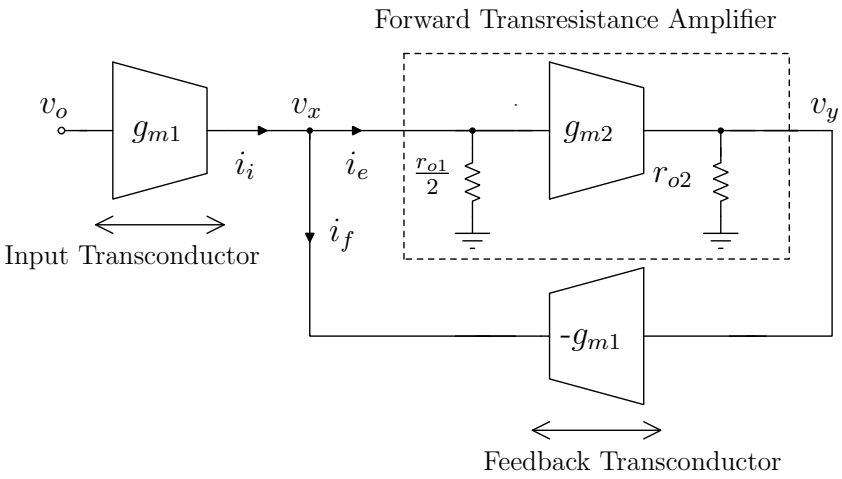


Figure 4.4: Model of the attenuator under DC operating conditions.

$$\begin{aligned} Z_{cl} &= \frac{Z_{ol}}{1 + R_{ol}G_f} \\ &= \frac{\frac{r_{o1}}{2}}{1 + \frac{g_{m2}r_{o2}g_{m1}r_{o1}}{2}} \end{aligned} \tag{4.3}$$

Since the loop gain is very large Z_{cl} can be approximated as follows,

$$Z_{cl} \approx \frac{1}{g_{m2}g_{m1}r_{o2}} \tag{4.4}$$

Therefore,

$$v_x = v_o \times g_{m1}Z_{cl} \approx \frac{v_o}{g_{m2}r_{o2}} \tag{4.5}$$

$$v_y = g_{m2}r_{o2} \times v_x \approx v_o \tag{4.6}$$

From (4.5), attenuator gain $\alpha = \frac{v_x}{v_o} = \frac{1}{g_{m2}r_{o2}}$. If the product $g_{m2}r_{o2}$ is made equal to $g_{mc}r_o$ the output resistance of the main transconductor can be made infinite, as per (4.2). Another point to be noted is that, if g_{m2} and r_{o2} are made to track g_{mc} and r_o respectively across PVT, variation in DC gain across PVT will be similar to that of basic transconductor and is least affected by the r_o enhancing circuit. Since r_o

comprises of output resistance of both g_m and g_{mc}, it is necessary to make r_{o2} also to have a similar composition. This can be easily achieved by integrating the transconductor g_{mc} into the main transconductor g_m as shown in Figure 4.5. The transistors M_0 and M_1, in the figure, realize differential transconductance g_m while transistors M_5 and M_6 realize g_{mc}. For the transconductor g_{m2}, a replica of the transconductor shown in Figure 4.5 or its scaled version can be used, but with gates of M_0 and M_1 set at common-mode. This arrangement ensures $g_{m2}r_{o2} = g_{mc}r_o$.

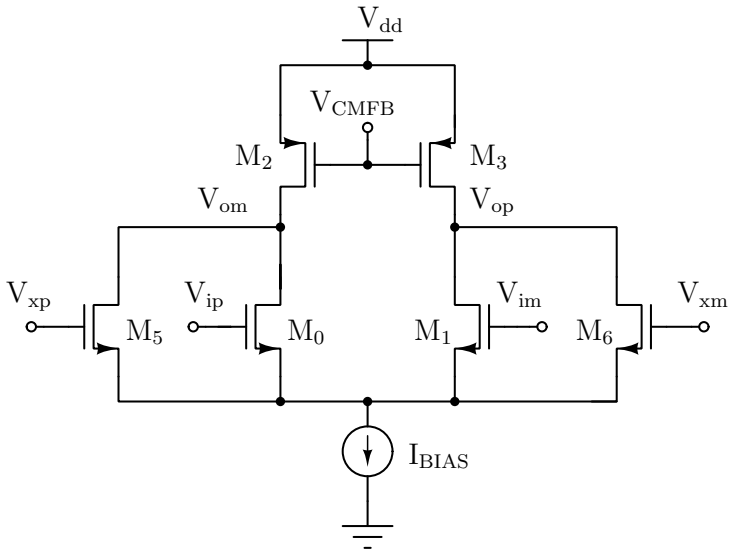


Figure 4.5: Schematic of the main transconductor g_m with g_{mc} integrated to it.

For the approximation in (4.5) to be accurate, it is desirable to have the loop gain $\frac{g_{m2}r_{o2}g_{m1}r_{o1}}{2}$ as large as possible. Larger the loop gain, better will be the enhancement in r_o. It is interesting to see in (4.5) that the linearity of the attenuator is predominantly decided by g_{m2}. Since the swing at the node v_x is small, the loop acts as a linear attenuator. A very small swing of v_x applied to g_{mc} in Figure 4.2 makes the current supplied by it also linear for relatively large output voltage swing. Therefore, the enhancement in DC gain of the main transconductor is desensitized to its output voltage swing to a large extent.

It can be noted that the approximation in (4.4) has an error that is inversely proportional to $1 + R_{ol}G_f$. In other words, the enhancement in DC gain that can be achieved is limited to the loop gain of the attenuator, $1 + R_{ol}G_f$ i.e. $1 + \frac{g_{m2}r_{o2}g_{m1}r_{o1}}{2}$. Higher loop gain can be achieved by choosing g_{m1} to have a large DC gain. A telescopic architecture can be used for realizing g_{m1}. Since the swing at node v_x is negligibly

small, head-room requirement for the telescopic amplifier is quite relaxed.

The gyrator loop in Figure 4.3, has two open loop LHP poles at $\frac{1}{r_{o2} \cdot C_{o2}}$ and $\frac{2}{r_{o1} \cdot C_{o1}}$, where C_{o2} and C_{o1} are parasitic capacitances at nodes v_y and v_x respectively. In addition, each of the two transconductors g_{m2} and $-g_{m1}$, contribute one RHP zero due to gate-to-drain capacitance in these transconductors. Since the gyrator loop is designed to have very large loop gain, it is necessary to compensate the gyrator loop against instability.

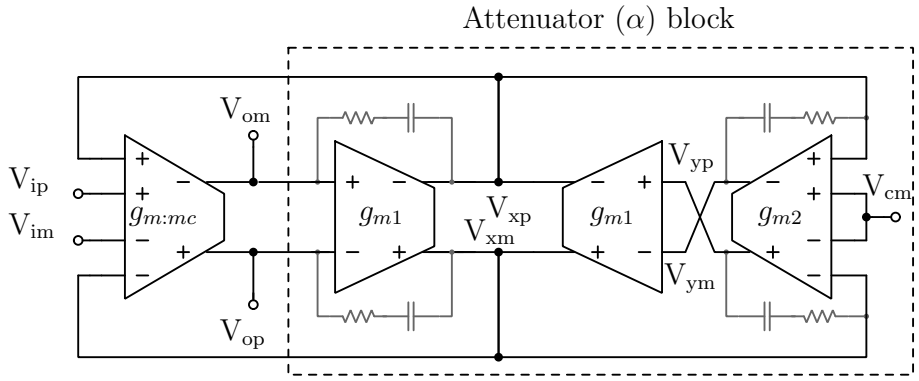


Figure 4.6: Complete schematic of the fully differential r_o enhanced transconductor

Figure 4.6 shows the schematic of fully differential r_o enhanced transconductor. The transconductor named $g_{m:mc}$ is a dual-input fully differential transconductor, the schematic of which is shown in Figure 4.5. The transconductor g_{m2} is the scaled down version of the transconductor $g_{m:mc}$ with a scaling factor of 2. The transconductor g_{m1} is realized using a fully differential telescopic OTA. The resistor and capacitor arrangement across g_{m1} and g_{m2} are used for compensating the loop.

4.4 Effect of common mode voltage mismatch

The common mode voltage of the main transconductor has a direct effect on the output impedance seen. Any mismatch in the common mode voltage results in a difference in the r_o matched, as the mirror transconductor sees a different r_o from that of the r_o present in the main transconductor. Therefore it becomes necessary to match the common mode voltage of the mirror transconductor in the attenuator loop, figure 4.3, to that of the main transconductor. In order to do so, make the dummy transistors (M_0 and M_1) in the mirror transconductor track the input common mode of the main

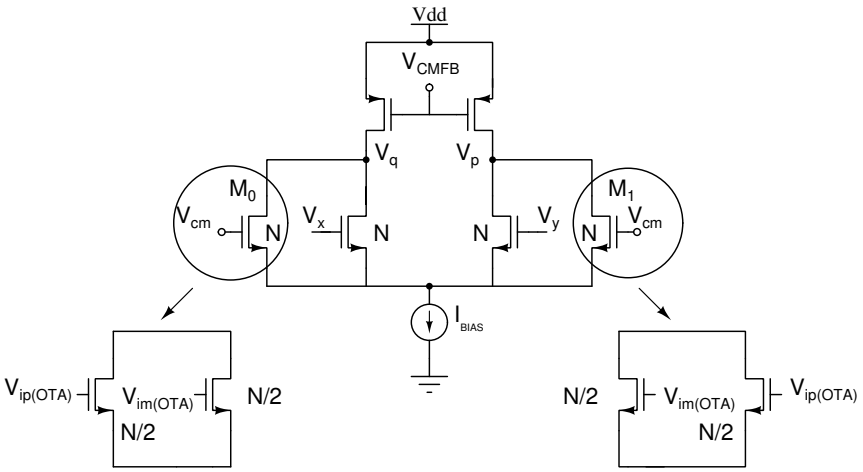


Figure 4.7: Splitting of dummy transistors to match common mode

transconductor. This is achieved by splitting the dummy transistors as shown in Figure 4.7.The inputs to the split dummies are given from the inputs to the OTA. The two dummies only allow the common mode current, canceling any differential current. Hence the input common mode voltage from the main transconductor is copied to the mirror transconductor in the attenuator loop. With better matching of the common mode voltages, the gain of the OTA doesn't degrade.

4.5 Simulation Results

The proposed scheme is validated in 0.18 μm CMOS technology from UMC technologies. The frequency response of the OTA with and without r_o enhancement has been compared.

Figure 4.8 shows the schematic of r_o enhanced OTA with additional compensation for stability. Main transistors of the transconductor are operated in weak inversion region to have low transconductance (12 nS) with a bias current of 10 nA.

The magnitude and phase response of the OTA with 10 pF load is shown in Figure 4.9 and 4.10 along with the frequency response of the basic OTA.

It can be seen that about 101.3 dB DC gain can be obtained by enhancing r_o of the basic transconductor. However, for the OTA without enhancement (with V_{xp} and V_{xm} set to small signal ground), the DC gain offered is 54.43 dB. Owing to the large loop gain of 46.9 dB offered by the attenuator loop, the DC gain of basic OTA is

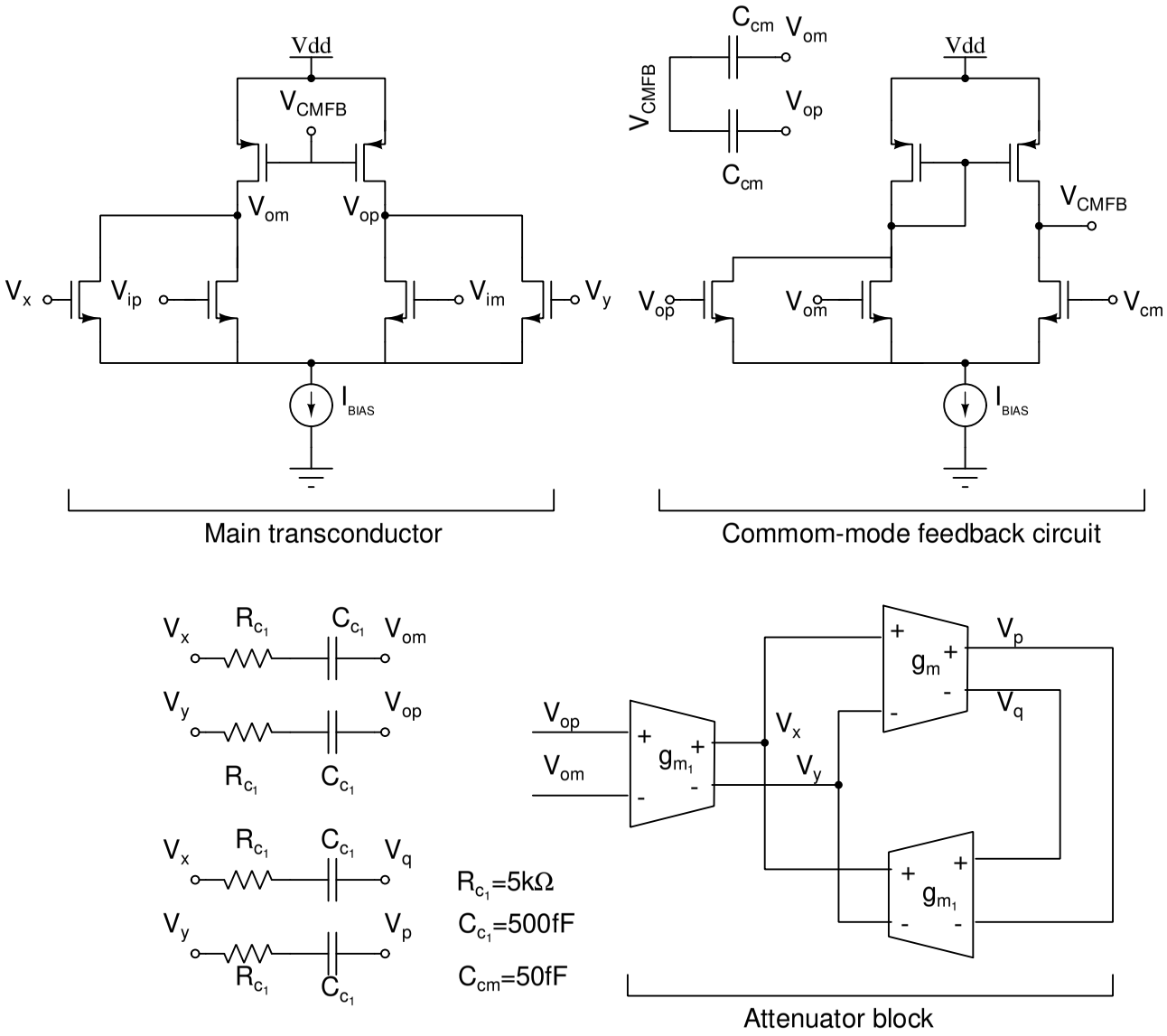


Figure 4.8: r_o enhanced OTA

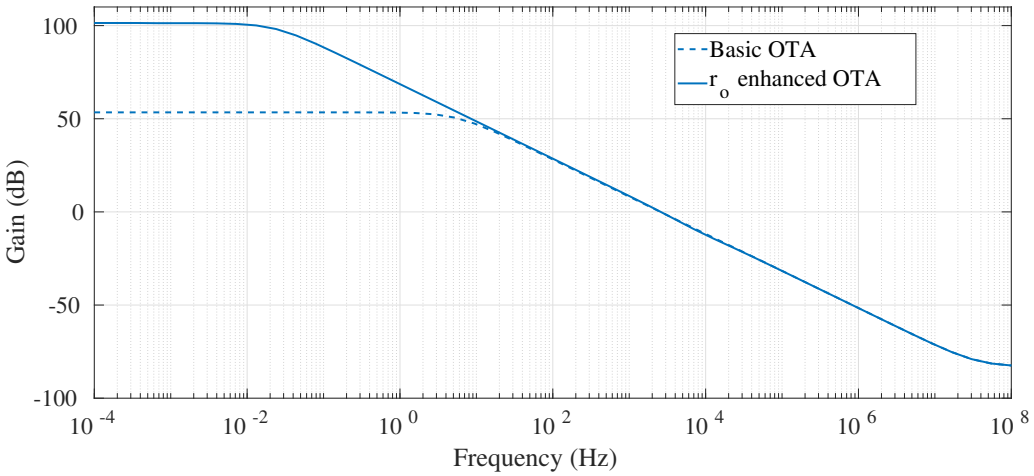


Figure 4.9: Comparison of Magnitude response of r_o enhanced OTA to basic OTA, ($C_L = 10\,\text{pF}$).

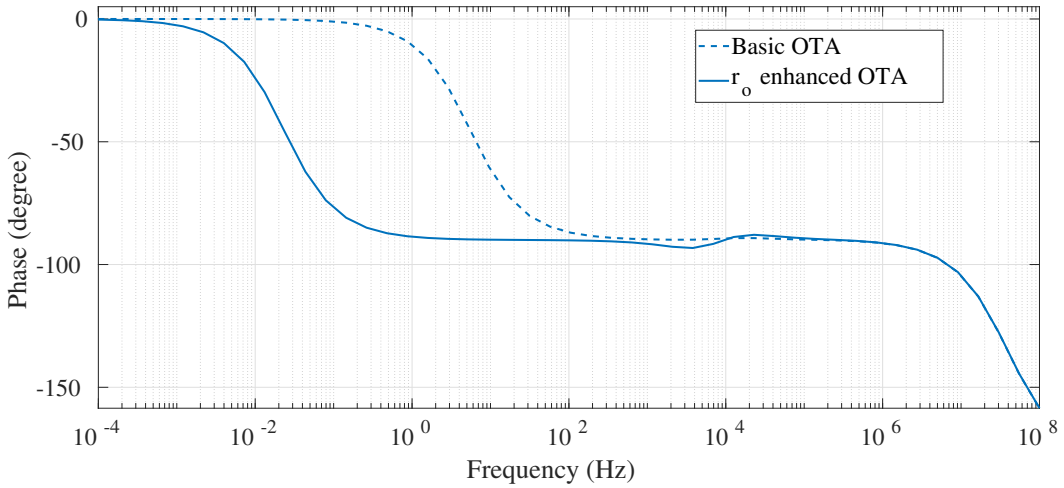


Figure 4.10: Comparison of Phase response of r_o enhanced OTA to basic OTA, ($C_L = 10\,\text{pF}$).

enhanced to 101.3 dB. It is to be noted that Miller compensation has been used for both proposed OTA and basic OTA. Both basic and r_o enhanced OTA offers a phase margin in excess of 87°.

Figure 4.11 shows the transfer characteristics of the OTA. The OTA is found to offer a good linearity up to about 1 V peak-to-peak input differential swing. Figure 4.12 shows the plot of DC gain versus output voltage swing of the OTA. The OTA offers a DC gain of 101.3 dB for an output voltage swing of ±0.57 V which is sufficient for

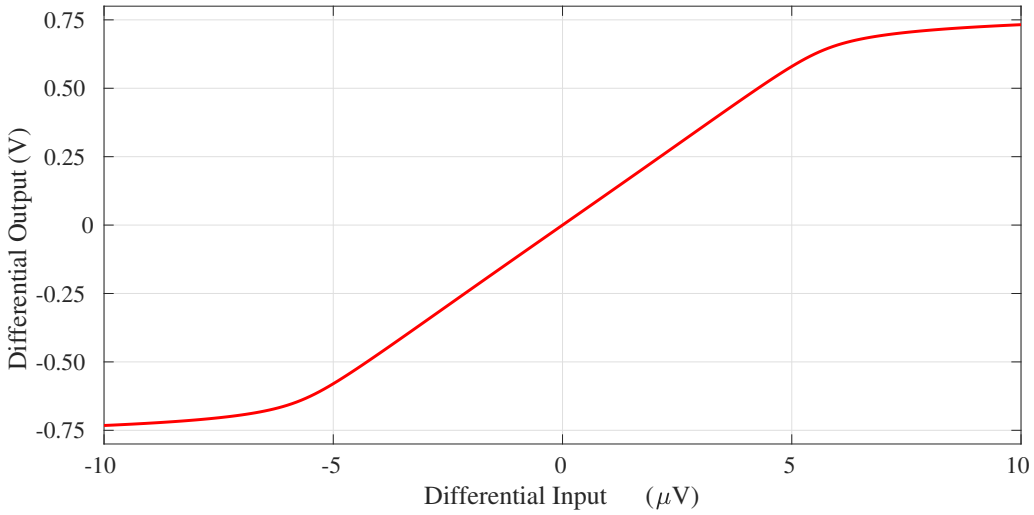


Figure 4.11: Transfer characteristics of r_o enhanced OTA.

biomedical applications.

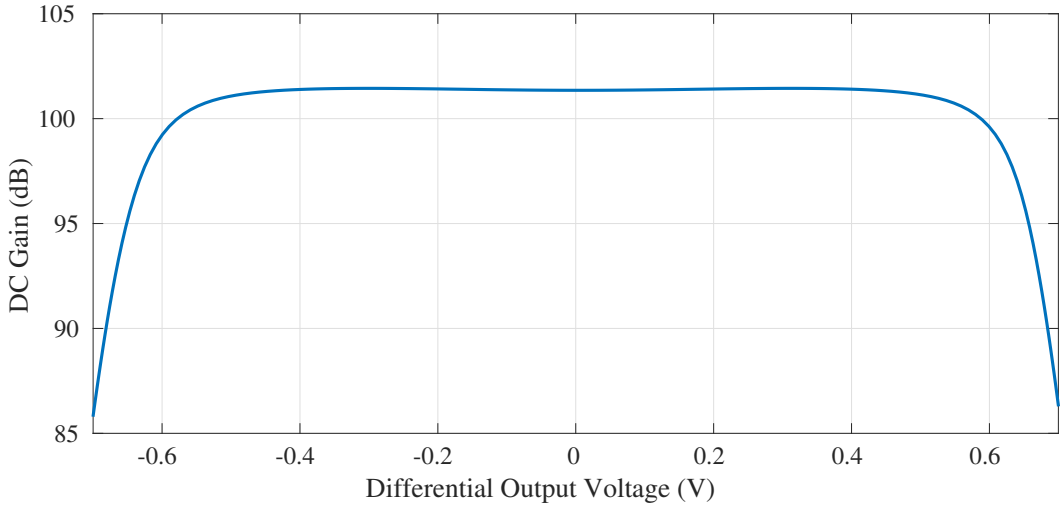


Figure 4.12: DC gain vs Output Voltage Swing

Table 4.1 compares the characteristics of basic OTA (without enhancement) to the r_o enhanced OTA. It can be observed that there is 46.9 dB boost in the DC gain, with little effect on other characteristics such as linearity, unity gain bandwidth etc. Also the phase margin is not affected by the enhancement.

Figure 4.13 and Figure 4.14 compares the variations in DC gain of the proposed

Table 4.1: Characteristics of OTA at 1.8 V Supply in UMC 180 nm Technology, (C_L = 10 pF).

	Basic OTA	r_o enhanced OTA
Supply Voltage (V)	1.8	1.8
Technology (μm)	0.18	0.18
Power (nW)	180	648
DC Gain (dB)	54.43	101.35
f_{-3dB} (Hz)	5.5	23m
f_u (kHz)	2.67	2.63
Linearity @1 % THD $V_{o,diff,pk-pk}$ (V) @$\frac{f_{-3dB}}{3}$	1.1	1.15
IRN (μV_{rms}) (1 mHz–10 kHz)	33.9	62.7
Phase Margin (°)	89.89	87

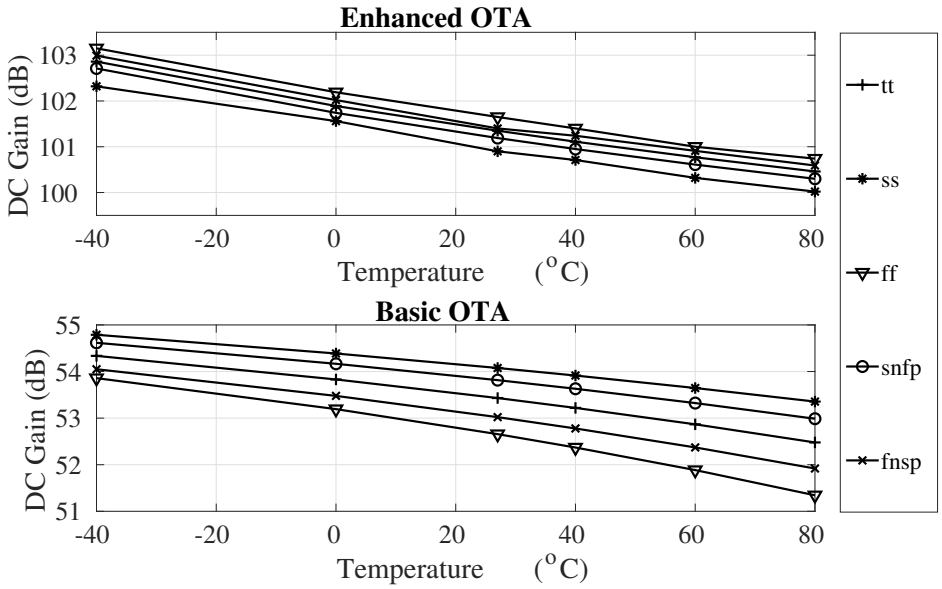


Figure 4.13: Variation of DC gain of r_o enhanced OTA compared to basic OTA vs Temperature.

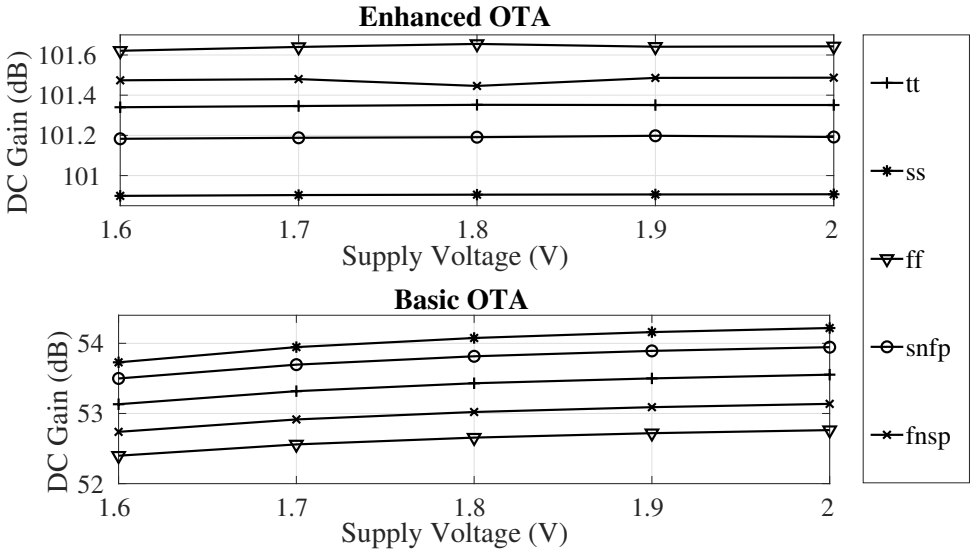


Figure 4.14: Variation of DC gain of r_o enhanced OTA compared to basic OTA vs Supply voltage.

OTA with the basic OTA across PVT variations. The observations are tabulated in Table 4.2. The table also compares the performance of this OTA with similar r_o enhanced OTAs found in literature. It can be seen that the proposed method offers least sensitivity of reduction in DC gain to output voltage swing without any need of dedicated tuning circuit.

A low sensitivity of the DC gain across PVT is due to the architecture where g_{m2} and r_{o2} are made to track g_{mc} and r_o respectively as explained in section 4.3.

Table 4.2: Performance comparison with related works.

	Yan and Geiger (2002)	Huang and Chen (2014)	This Work
CMOS Process	0.5 μm	0.13 μm	0.18 μm
Supply Voltage (V)	3	1.5	1.8
Current Consumption (A)	15m	1.12m	0.36μ
DC gain boost (dB) at $v_{out} = 0$	-	26.4	46.9
Output Swing Range (OSR) (V)	-0.24– 0.24	-1.1–1.1	-0.57–0.57
Reduction in DC gain boost (dB) over OSR	33	1	0.87
Sensitivity of gain boost to OSR (dB/V)	68.75	0.77	0.75
Minimum DC gain boost (dB) over temperature	-	23.2 (-40–80 °C)	45.6 (-40–80 °C)
Minimum DC gain boost (dB) over supply voltage	-	21.1 (1.3–1.8 V)	46.7 (1.6–2 V)
Calibration of tuning circuits	high gain, low offset, comparator	NA	NA

4.6 Filter Design Using the r_o Enhanced Transconductor

The concept of conductance cancellation scheme is applied to the cross-coupled differential pair transconductor proposed in Chapter 2 to achieve high r_o. The reason is with g_m cancellation technique adopted for realizing very low transcondutance, it is interesting to check whether the proposed r_o enhancement scheme can readily be applied.

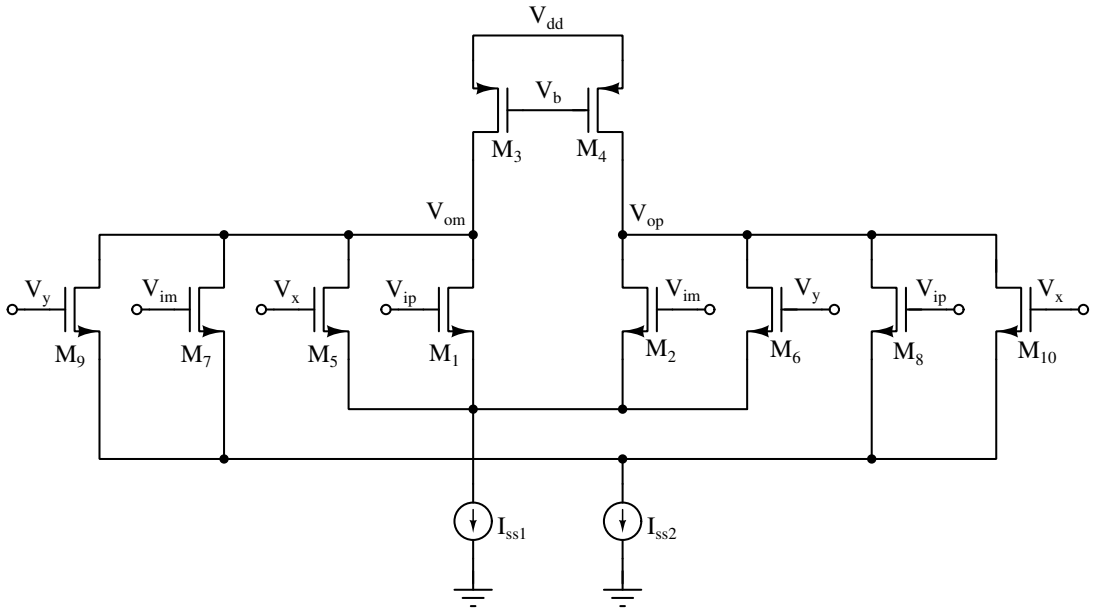


Figure 4.15: Cross-coupled transconductor

The cross-coupled differential pair shown in Figure 2.2 is required to be modified as shown in Figure 4.15. However, here a NMOS realization is adopted. The transistors M_1, M_2, M_7 and M_8 form the basic input stage and transistors M_5, M_6, M_9 and M_{10} are feedback transistors realizing g_{mc}. All the transistors are sized equal and are operated in sub-threshold region. The two differential pairs have tail currents I_{ss1} and I_{ss2}, and $I_{ss1} \approx I_{ss2}$ such that $I_{ss1} - I_{ss2} = \Delta i$. The cross coupled arrangement of the two differential pairs effectively offers a low transconductance as explained in the section 2.2.

To achieve low transconductance, the two currents I_{ss1} and I_{ss2} are to be generated such a way that they have a very small difference Δi. A modified architecture based

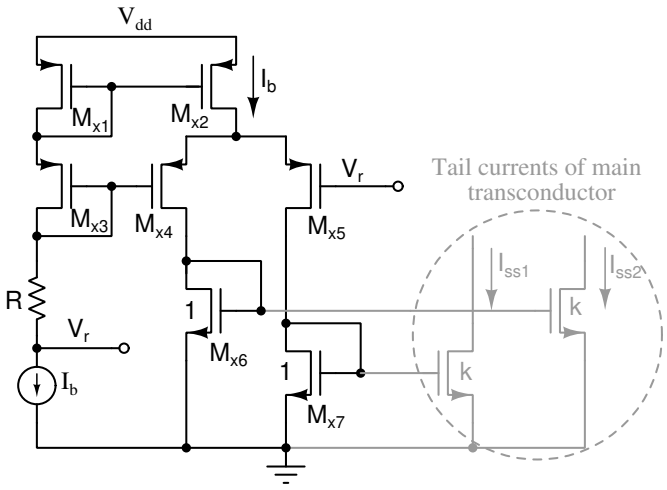


Figure 4.16: Tail currents generation circuit

on the circuit proposed in section 2.2.1 is used to generate tail currents I_{ss1} and I_{ss2} with a tunable difference of Δi. The scheme proposed to achieve this is shown in Figure 4.16.

The r_o of the transconductor is enhanced by using the proposed scheme explained in 4.3. The common-mode feedback (CMFB) circuit shown in Figure 4.8 is used to set common mode voltage levels of the output node.

A first order fully differential low-pass filter g_m-C is realized using the r_o enhanced cross-coupled differential transconductor. The schematic of the filter designed in UMC 0.18 μm CMOS technology is shown in Figure 4.17.

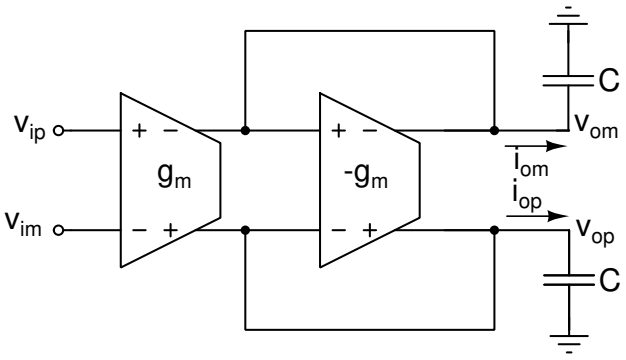


Figure 4.17: First-order fully differential $g_m - C$ filter.

Figure 4.18 shows the magnitude response of the filter. The filter bandwidth is tuned by varying the resistor R. The tuning range achieved is from 0.5 Hz to 10 Hz, for

I_b=1 nA, C=50 pF and R= 500 kΩ to 10 MΩ. The tuning range is increased from 10 Hz to 365 Hz by increasing the bias current I_b=10 nA for the same capacitor and resistor values. An off-chip resistor (potentiometer) is preferred for R, over on-chip resistor, as it is required to be tuned. The proposed resistor based tuning (R-tuning) scheme in section 2.2.1 has a limited tuning range. The tuning range is limited by the output impedance and reduction in DC gain on the lower frequency side. By enhancing the r_o of the transconductor, the cut-off frequency is further reduced without the reduction in DC gain.

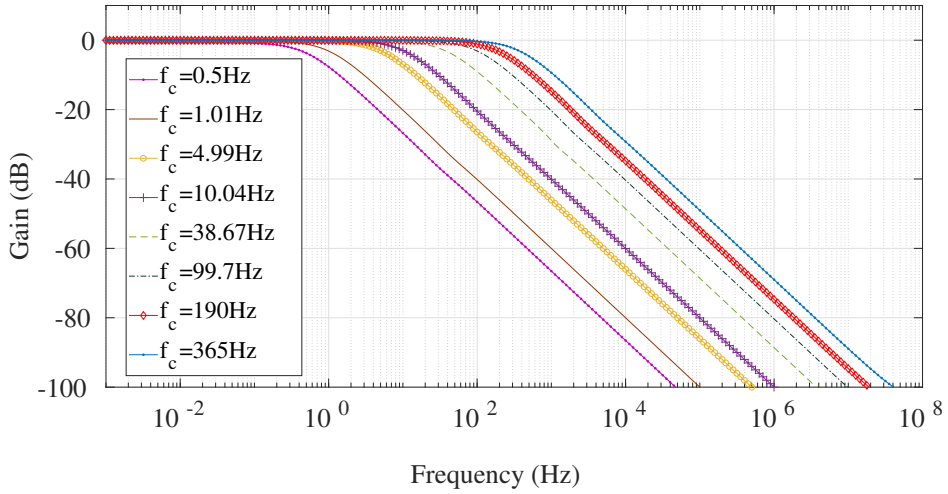


Figure 4.18: Magnitude response of the filter for R tuning. The tuning range is from 0.5 Hz to 365 Hz. The settings used for these results are in the format [Bias current I_b, resistor value, cutoff frequency]: [1 nA, 500 kΩ, 0.5 Hz], [1 nA, 1 MΩ, 1 Hz], [1 nA, 5 MΩ, 4.99 Hz], [1 nA, 10 MΩ, 10.04 Hz], [10 nA, 1 MΩ, 38.67 Hz], [10 nA, 3 MΩ, 99.7 Hz], [10 nA, 5 MΩ, 190 Hz] and [10 nA, 10 MΩ, 365 Hz].

Table 4.3 summarizes the filter performance. To evaluate the filter performance, two cases are considered.

- With I_b=1 nA (f_c=10 Hz setting). The filter is excited with sinusoidal signal of amplitude 264 mV_{pp} differential at 1 Hz. A total harmonic distortion (THD) of 1 % is obtained. With an in-band (0.1 Hz to 10 Hz) input-referred noise (IRN) of 175.76 μV_{rms}, the filter is found to offer a dynamic range (DR) of 54.50 dB. It is to be noted that the total power consumed by the filter is 0.207 μW operating on 1.8 V supply.

- With I_b=10nA (f_c=100 Hz setting). A total harmonic distortion (THD) of 1 % is obtained for a input sinusoidal signal of amplitude 312 mV_{pp} differential at 10 Hz. The filter is found to offer a dynamic range (DR) of 59.29 dB for an in-band (0.1 Hz to 100 Hz) input-referred noise (IRN) of 119.70 μV_{rms}. The total power consumed by the filter is 1.44 μW operating on 1.8 V supply.

Table 4.3: Summary of the filter performance at 1.8 V Supply.

PARAMETERS	Value (I_b = 1nA)	Value (I_b = 10nA)
Current consumption (μA)	0.115	0.803
Power (μW)	0.207	1.44
DC Gain (dB)	0	0
Filter Order	1	1
Bandwidth (Hz)	10 Hz	100 Hz
Linearity @1 % THD ($V_{in,pk-pk}$ (mV))	264	312
IRN (μV_{rms})	175.76 (100 mHz–10 Hz)	119.70 (100 mHz–100 Hz)
Dynamic range (dB)	54.50	59.29

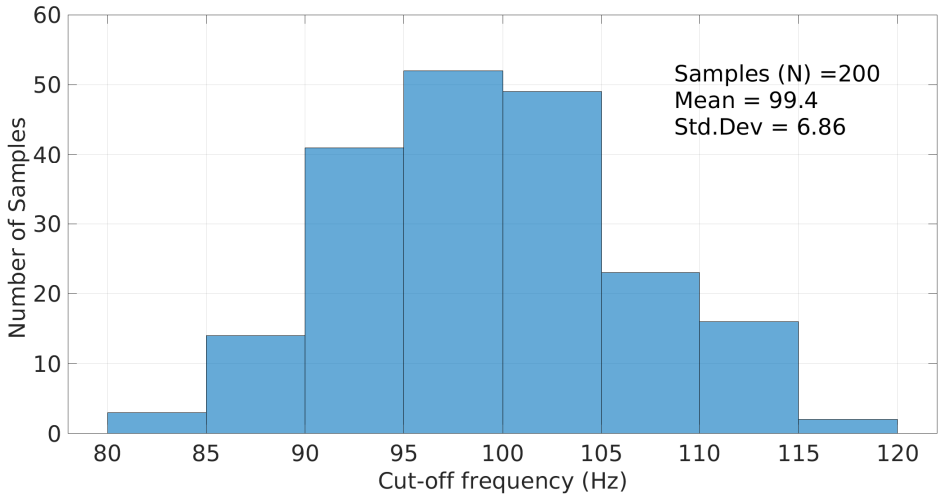


Figure 4.19: Monte-carlo simulation of the filter with 200 runs for f_c = 100 Hz setting.

Monte-carlo simulations are performed to evaluate the performance of filter (f_c=100 Hz setting) for device process variations and mismatch. Mean of about 99.4 Hz and stan-

dard deviation of about 6.86 Hz is observed without the use of any bandwidth fixing loop. The distribution of cut-off frequency is shown in the Figure 4.19.

Simulations are carried out across process corners, supply voltage and temperature (PVT) variations, for a setting of f_c=100 Hz.

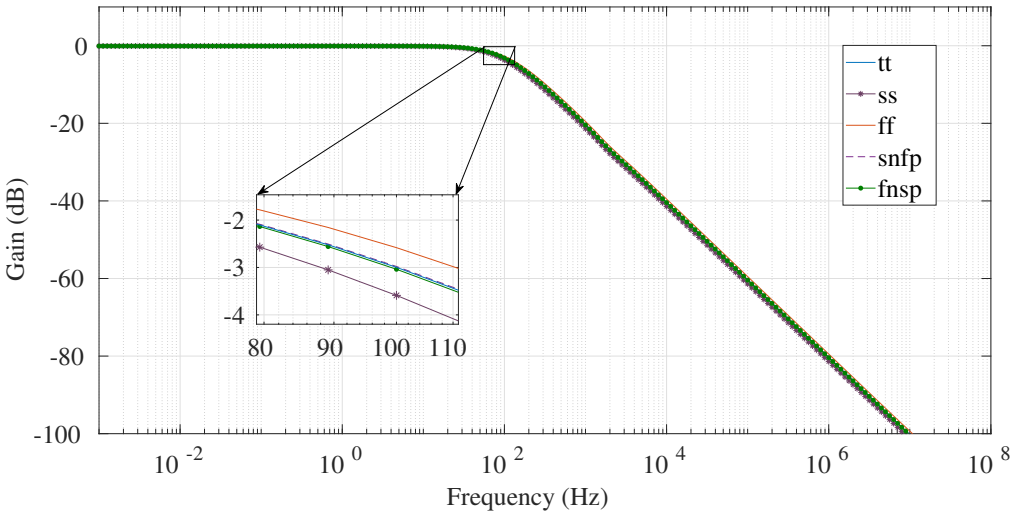


Figure 4.20: Magnitude response of the filter across various process corners at room temperature.

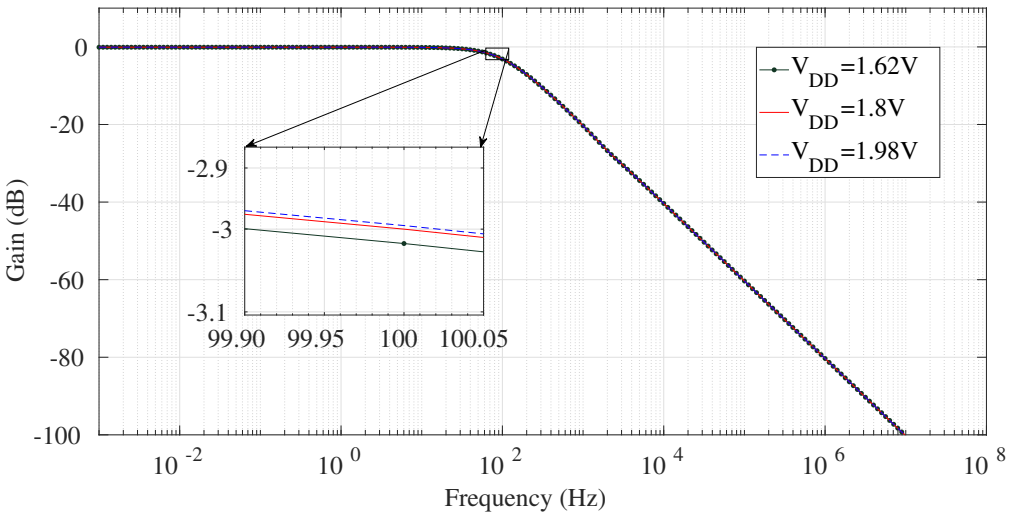


Figure 4.21: Magnitude response of filter for 10% change in supply voltage at typical corner and room temperature.

The magnitude response of the filter at different process corners is shown in Fig-

ure 4.20. The change in cut-off frequency f_c is less than 12% at nominal supply voltage of 1.8 V and at room temperature (27°C). Figure 4.21 shows the magnitude response for ±10% variation in supply voltage from the nominal value at room temperature and at typical process corner. The change in bandwidth is less than 1%. For variation in temperature from 0°C to 80°C at typical corner and nominal supply voltage, the bandwidth variation is less than 15% as shown in Figure 4.22. These deviations can be tuned back by re-adjusting R appropriately.

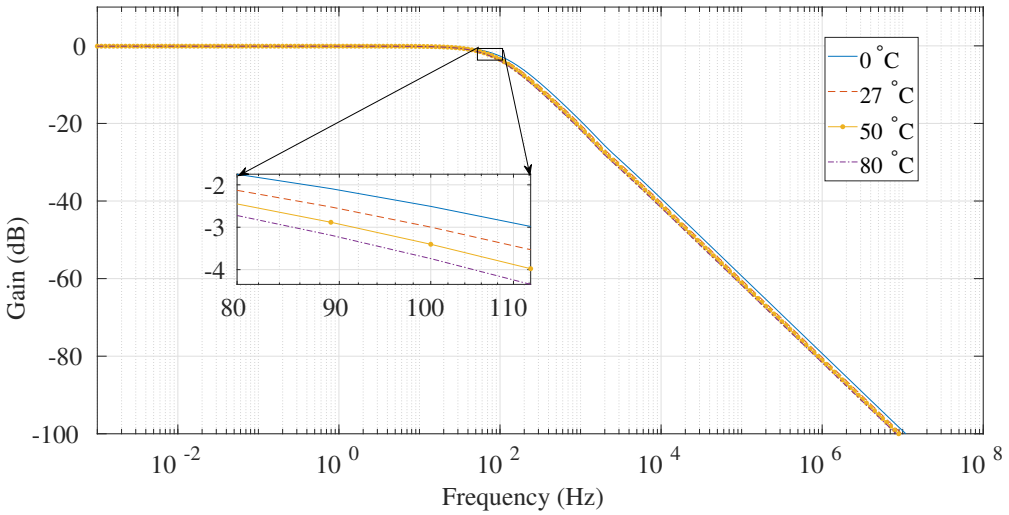


Figure 4.22: Magnitude response of the filter for change in temperature $(0 - 80^{o}\text{C})$ at typical corner and nominal supply voltage (V_{DD}=1.8 V).

Chapter 5

CONCLUDING REMARKS AND FUTURE WORKS

5.1 Conclusions

A novel technique is proposed to reduce g_m for realising low frequency g_m - C filters. A technique to tune the effective transconductance is also presented. The proposed technique has been validated through simulations by designing a fourth-order low-pass Butterworth filter using transconductor cells. The architecture of g_m -cell makes it possible to realise a fully differential filter without the need for an explicit CMFB circuit. The simulation results justified that the proposed tuning scheme is linear. A tuning range of 1-100 Hz was achieved. The tuning range has been increased to 30 mHz-100 Hz by using a switched g_m -cell and modifying the filter circuit accordingly.

The ultra low power, second order, switched sub-threshold source follower biquad based filter proposed in this thesis best in its class with a dynamic range of 91.86 dB. Switching technique used for the filter allowed the adjustment of cut-off frequency in the range 4 Hz to 100 Hz. The filter exhibited a very good FoM when compared to the state-of-the-art filters.

A novel gyrator based output conductance cancellation method to boost the DC gain of a differential amplifier proposed is capable of boosting the DC gain of a simple transconductor by about five orders of magnitude. The concept and the associated design is simple to realize. The scheme is found to offer a minimum enhancement of 45 dB across PVT variations. Overall, the OTA is found to offer 0.75 dB/V sensitivity of gain boost over OSR, which is the least among similar schemes found in literature.

A first order filter designed using the proposed OTA is able to offer cut-off frequency down to 0.5 Hz without any switching scheme, and more significantly without the loss of DC gain.

All proposed filters are capable of extracting most bio potential signals because of wide tunable bandwidth. All the proposed filters are proved to be robust with encouraging Monte-Carlo simulations. In addition, the low power architecture make these filters highly suitable for use in portable bio-medical instruments.

5.2 Future Works

One of the issues in designing g_m-C filters is to ensure the filter performance as per specifications across PVT variations and transistor mismatches. Usually for g_m-C filters designed to operate in weak inversion region the bandwidth varies upto $\pm 20\%$ for PVT Variations and mismatch. An automatic tuning circuit is the most commonly used scheme in integrated filters for correcting the variations in bandwidth. In thesis, the emphasis was more towards proposing new architectures for low frequency filters and proving their candidature in bio-medical applications. Therefore, not any significant effort has been made towards automatic tuning of bandwidth. It will be quite interesting to design an automatic tuning circuit for proposed transconductor and filter architectures.

The recent trend in the design of low frequency filters is to use single branch filters. Most widely used architectures to implement single branch filters are source followers. The source follower based filters are best suited for biomedical applications, as they are more power-efficient when compared to conventional g_m-C filters. Design of source follower based filter architectures can be explored further.

Using the r_o enhanced transconductor as the first stage, a two stage OTA design can be attempted with common-source amplifier used as second stage. With the use of common-source amplifier at the second stage, the DC gain can be potentially increased to 150 dB or beyond. However, it could be an interesting problem to address on the stability front.

Designing low power filter circuits for biomedical applications in the era of Internet-of-things could be quite challenging. Therefore, the scope of research in designing such circuits is never-ending. Any analog circuit which can be thought for low power applications, is worthwhile to be tried.

Appendix I
PERFORMANCE METRICS

A-1 Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is a measurement used to estimate the system non-linearity. It tells the amount of distortion present in the output signal due to harmonics. Total harmonic distortion (THD) is defined as the ratio of sum of the powers of all harmonics to the power of the fundamental frequency. Total harmonic distortion is usually expressed in terms of percentage or in decibels (dB) relative to the fundamental component as distortion attenuation.

$$THD\,(dB) = 10\,log\left(\frac{P_2 + P_3 + P_4 + ...}{P_f}\right) \tag{A.1}$$

where P_2, P_3 and P_4 are the powers of 2^{nd}, 3^{rd} and 4^{th} harmonics respectively. P_f is the power of fundamental. THD is also defined as

$$THD\,(dB) = 20\,log\left(\frac{\sqrt{V_{rms2}^2 + V_{rms3}^2 + V_{rms4}^2 + ...}}{V_{rmsf}}\right) \tag{A.2}$$

where V_{rms2}, V_{rms3} and V_{rms4} are the rms voltages of 2^{nd}, 3^{rd} and 4^{th} harmonics respectively. V_{rmsf} is the rms voltage of fundamental.

Lower THD value indicates less distortion in the system output. The quality of filters is often specified using THD. A filter with THD of 0.01 or lower ($\leq$ 1%) is considered to be normal. In dB, 1% THD corresponds to -40 dB. In literature, most of the filters are designed to have THD of $\leq$ 1%.

A-2 Power Consumption

Power consumption is one of the key parameter to be considered while designing the circuits for biomedical systems. Low power circuits are highly important in the following kind of systems:

1. Portable systems operated with battery
2. Energy harvesting systems or sensors
3. Low cost systems
4. Low heat dissipation systems

Typically, portable systems are of smaller size operated with batteries. To increase the lifetime of batteries or to reduce the time between recharges, the circuits designed should consume low power. The power constraint becomes more stringent for more miniature systems. Energy harvesting systems can accommodate circuits only with low power consumption as they survive on the small amounts of energy derived from their surroundings. Low power consumption is important for reducing the cost of overall system as the cost of the battery increases with size, increasing the overall cost.

Biomedical systems are examples of such systems where low power circuits is extremely important. If the circuits are for wearable and implantable biomedical devices, then the design must consume low power to reduce the amount of heat dissipated, so that human tissues surrounding the devices will not be damaged, and also to increase the battery life and reduce the battery size and overall weight. This is because using of bulk batteries and frequent replacement of batteries is not practical. If the design is not for wearable and implantable devices then the constraint on power consumption can be relaxed.

The total power consumption of filter is the product of supply voltage and sum of currents through all the branches in the circuit. Designing filter circuits to consume low power by preserving linearity, noise and dynamic range is quite challenging.

A-3 Bandwidth

One of the most significant aspects of biomedical filters is bandwidth. Specifically, bandwidth in filters is often referred to the passband bandwidth. For low-pass filter, passband bandwidth is frequency range between 0 and the -3 dB point of the filter

magnitude response. For most of the filters in biomedical systems, the requirement in bandwidth is <100 Hz. The 3 dB bandwidth in $g_m - C$ filters is given by g_m/C. Low bandwidth (or low cut-off frequency) is practically achieved by reducing g_m.

In biomedical systems, A filter with tunable bandwidth, that extracts most bio potential signals is widely preferred to enhance the re-usability of the filter and for cost minimization.

A-4 Noise

Noise is the paramount parameter in circuits designed for biomedical applications. Since the bio-electric signals are of low amplitude the circuits must exhibit low input-referred noises to process the weak signals precisely. The common noise contributors of mos devices are thermal noise and flicker noise.

In MOS devices, random fluctuation of mobile carriers in the channel due to thermal excitation causes thermal noise. Thermal noise can be modelled by a drain to source connected current source as shown in Fig. A.1 with spectral density (Razavi 2005)

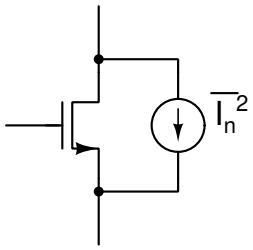


Figure A.1: MOSFET thermal noise

$$\overline{I_n^2} = 4kT\gamma g_m \tag{A.3}$$

where k is the Boltzmann constant, T is the absolute temperature, coefficient $\gamma \approx 1$ and g_m is the transconductance of transistor.

The main cause of Flicker noise in MOS devices is due to random trapping of the charge carriers in the channel and gate oxide. The flicker noise of the MOS transistor is given by Razavi (2005)

$$\overline{I_{n,f}^2} = \frac{K_f}{C_{ox}WL} \cdot \frac{g_m^2}{f} \tag{A.4}$$

where K_F is a parameter that depends on transistor dimensions, C_{ox} is oxide capacitance, W, L are width and length of the transistors, g_m is the transconductance of transistor and f is the frequency. In filter circuits noise is due to both thermal noise and flicker noise. The circuits designed for bio-electric signals are highly susceptible to flicker noise (1/f noise) due to their low frequency of operation and also flicker noise is the dominant noise contributor. Fig. A.2 shows the importance of 1/f noise at low frequencies when compared to the thermal noise.

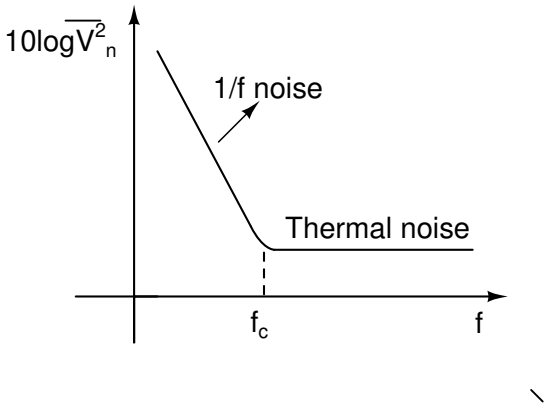


Figure A.2: Noise plot where spectral density is dominated by flicker noise (1/f) noise at low frequencies less than f_c.

From (A.4), flicker noise of a transistor is inversely proportional to its W-L product (gate area). By increasing the gate area of the transistors to sufficiently large value, the flicker noise can be suppressed to a sufficiently low value.

For bio-medical filters, the requirement on inband input referred noise of the filter for a given input voltage and SNR is given by (Lee and Cheng 2009)

$$Noise_{in,ref}(rms) \leq \frac{V_{in,rms}}{10^{SNR(dB)/20}} \tag{A.5}$$

If the noise contributed by the filter is well within the range it doesn't cause any significant performance degradation. Normally, input referred noise is considered for representing the circuit noise. Input-referred noise indicates the amount of input signal corrupted by noise, i.e., it indicates the minimum signal that can be detected by the circuit with acceptable signal-to-noise ratio. It also helps in the fair comparison of noise performance of the designed filter with different filter circuits.

A-5 Dynamic Range (DR)

Dynamic range is defined a the ratio of highest signal level to the smallest signal level that a circuit can handle. Highest input is limited by the distortion and smallest input is limited by the noise. For analog filters, dynamic range is defined as

$$\text{Dynamic range} = \frac{\text{Power of input signal for a specified THD at the output}}{\text{Input referred noise power}} \tag{A.6}$$

To clearly distinguish between the desired signal and noise, high dynamic range filter circuits are needed.

A-6 Figure of Merit (FoM)

Figure of merit (FoM) is a metric used to compare the performance of various filters available in the literature. FoM combines several circuit parameters into a single value often helpful for comparison. FoM is defined by (Liu *et al.* 2012)

$$FoM = \frac{\text{P}}{\text{N} \times \text{DR}} \tag{A.7}$$

where P is the total power consumption, N is the filter order and DR is the dynamic range. Lower FoM indicates the better filter performance. FoM of a filter can be enhanced by designing the filter to consume low power for a given N and DR. Also, DR can be enhanced by designing the filter to have low distortion and noise which in-turn enhances the FoM.

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Appendix II
The Power-Efficient Weak Inversion Region of Transistor Operation

A-7 Introduction

Power is the product of supply voltage and current. Power can be reduced by operating the systems at lower voltages and/or currents. Power savings, by scaling the supply voltage is limited by the performance degradation of analog circuits. It is difficult to preserve the performance of circuits for supply voltages below 0.25 V. Thus scaling the currents is the promising option. In weak inversion or sub-threshold region of operation, transistors can be operated with low currents ranging from pA to μA. Transistor is operated in sub threshold region by choosing appropriate transistor dimensions and bias voltages.

The drain current of MOS transistor in sub-threshold region is given by

$$I_D = K I_{Do}\, exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right)\left(1 - exp\left(\frac{-V_{DS}}{\eta V_T}\right)\right) \tag{A.8}$$

where $K = W/L$ is the aspect ratio of transistor, μ is the carrier mobility, C_{ox} is the gate-oxide capacitance, $\eta = \frac{C_{ox}+C_{depl}}{C_{ox}} \approx 1.5$ is the sub-threshold slope factor, $V_T = \frac{kT}{q} \approx 26\,mV$ is the thermal voltage and V_{TH} is the threshold voltage. I_{Do} is the pre-exponential factor of sub-threshold current given by

$$I_{Do} = \mu C_{ox}(\eta - 1)V_T^2\, e^{-V_{TH}/(\eta V_T)} \tag{A.9}$$

For V_{DS}>$4V_T \approx 100\,mV$, (A.8) is reduced to

$$I_D = K I_{Do}\, exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \tag{A.10}$$

The transconductance of the MOS transistor in sub-threshold region is given by

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{\eta V_T} \tag{A.11}$$

Since g_m purely a function of I_D. The current I_D can be reduced, to achieve low g_m which also results in low power consumption. In this research, transistors are mainly designed to operate in the weak inversion region for achieving low-power consumption. In the weak inversion region of operation, it is important to design the circuits that are robust to noise, transistor mismatch, process and temperature variations.

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Bio-data

NAME : Jayaram Reddy M K

CONTACT DETAILS

Address : S/o M V Krishna Reddy, #77, 2^{nd} Cross,
Kuvempu Road, Muthyalpete,
Mulbagal, Kolar Dist., Karnataka–563131

☎ : 9886149041

✉ : jayaram.041@gmail.com

EDUCATIONAL QUALIFICATIONS

Doctor of Philosophy (Ph.D)

National Institute of Technology Karnataka, Surathkal 2014–Till date

Master of Technology (M.Tech)

Dr. Ambedkar Institute Of Technology, Bangalore 2009–2011

Branch : VLSI Design & Embedded systems

Bachelor of Engineering (B.E)

CMR Institute Of Technology, Bangalore 2004–2008

Branch : Electronics and Communication Engineering