Virtual Impedance based DFCL for DVR during Downstream Faults

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***Abstract*— This paper proposes a Downstream Fault Current Limiter (DFCL) for DVR during downstream faults. It Is based on the concept of Virtual Impedance (VI) which introduces the impedance in series to the system to suppress the large fault currents in the line. In the present work no additional equipment is involved for limiting the fault current and DVR itself is controlled such that FCL operation is ensured. The proposed VI based FCL features flexible implementation and can effectively suppress the fault current during the downstream faults and thereby the DVR is protected along with restoration of PCC voltages. Simulation studies are performed for 10 kV system using PSCAD/EMTDC platform and respective results are presented which proves the feasibility and efficacy of the proposed FCL.**

Keywords— Downstream fault, fault current limiter, virtual impedance, virtual inductance.

NOMENCLATURE

Z_s	Source Impedance
Z_l	Load Impedance
V_{line}	Line Voltage
V_{inj}	DVR injection voltage
V_{PCC}	PCC Voltages
V_s	Source Voltage
I_F	Fault Current
R_{line} &R_s	Line resistance and Source Resistance
L_{line} &L_s	Line Inductance and Source Inductance
R_f, L_f, C_f	Filter resistance, inductance and capacitance
k_{pv}, k_v	Co-efficients of proportional and resonant terms of voltage controller
Z_v	Virtual Impedance

I. INTRODUCTION

Today's modern world stepped into new era of technology which raised the quality of living but at the same time made dependent on usage of high sensitive and critical equipment which introduced power quality issues in the distribution system. Of these, problems related to voltage viz., sag, swell and harmonics are considered to be most important PQ problem. To overcome these issues a set of FACTS devices called custom power devices are being used. Among them Dynamic Voltage Restorer (DVR) [1] is widely used device to compensate the voltage disturbances in distribution system. The typical DVR installed system is shown in fig.1.

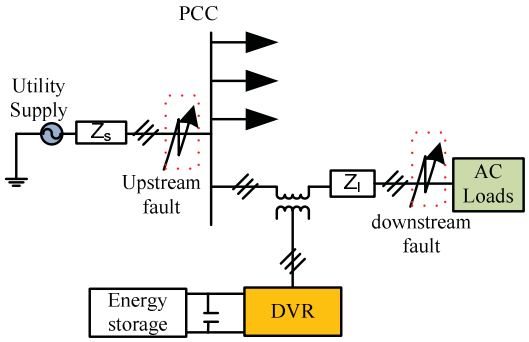

Fig.1 Typical DVR structure in distribution system

It consists of energy storage device, voltage source inverter, inverter output filter and series injection transformer.

Distribution systems are often prone to upstream faults i.e. faults on the source side as shown in fig.1. The main objective of DVR is to inject the voltage in series with line to maintain prefault voltage at load side. In literature [2]- [5] many control algorithms are proposed for efficient operation of DVR. Once the sag is detected then the control algorithm of DVR generates reference voltages of $V_{ref} = V_l - V_s$ where V_l is prefault load voltage and Vs is the post sag source voltage. The generated reference voltage is injected through series transformer into the line. Apart from the upstream faults the downstream faults are also often occurring event in the distribution systems. Unlike upstream faults the impact of downstream fault is very severe. For the system shown in Fig.1 if downstream fault occurs (on load side) causes high currents to flow into the system thereby the devices connected in the system are damaged and moreover causes drop in PCC voltages. Thus the loads connected to the other feeder are affected too. In [4]-[5] the DVR is accompanied by a mechanical bypass switch which will bypass DVR during the downstream fault conditions. Though this method protects the DVR but still the PCC voltages are not recovered. So controlling DVR to limit the fault current and at the same time to restore the PCC voltages was a promising approach. Recently the active control of DVR [6]- [8] is appearing as promising approach to limit the large fault current and restore the PCC voltage.

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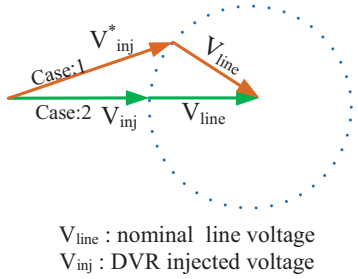

Fig.2. Phasor diagram of DVR operation during downstream fault

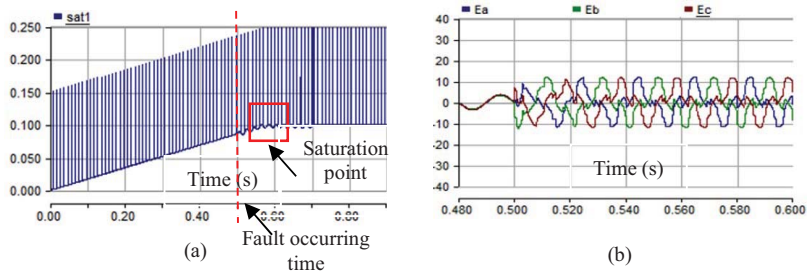

Fig.3 Limitations of flux-charge based FCL control algorithm (a) Saturation of flux, (b) DVR injected voltages

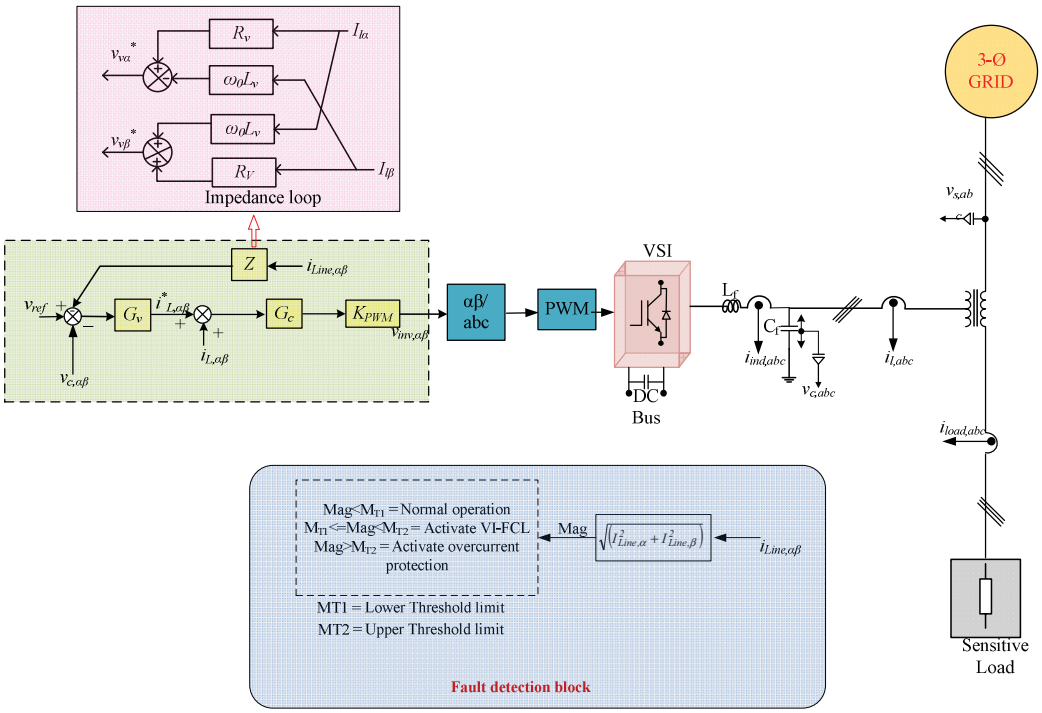

Fig.4 Control block diagram of virtual impedance based fault current limiter for DVR

In [9] DVR is controlled in such a way that it injects the reverse voltage in to the grid to limit the downstream fault current. But this method requires high rating of DVR which restricts the application of this method as the power capacity of the series connected device is only about 50% of load capacity. In [10] an additional reactor is added to the line but this method increase the voltage drop of the line when DVR is not operating. In [11] DVR is controlled as virtual inductor to limit the downstream fault currents but this method also posses its limitations (discussed in next section). So, in this paper a Virtual Impedance (VI) [12]-[14] based DFCL control algorithm is proposed for DVR to limit the flow of large fault currents, and to restore the PCC voltage as well. The VI-DFCL acts as virtual impedance in series with distribution feeder. Section-II describes the evolution of proposed DFCL and section-III presents the simulation results of proposed VI-DFCL based DVR system compensating downstream faults.

II. Control of DVR during Downstream Faults

In this subsection firstly the concept of using DVR to limit fault current during downstream fault is discussed and later followed by the description of proposed VI-DFCL control algorithm for DVR.

A. Operation of DVR during downstream faults:

In Fig.1 the fault at load side is considered as downstream fault scenario for the DVR connected system. The fault current and PCC voltages are calculated by using voltage divider concept and is given as

$$I_F = \frac{V_s}{Z_s + Z_l} \tag{1}$$

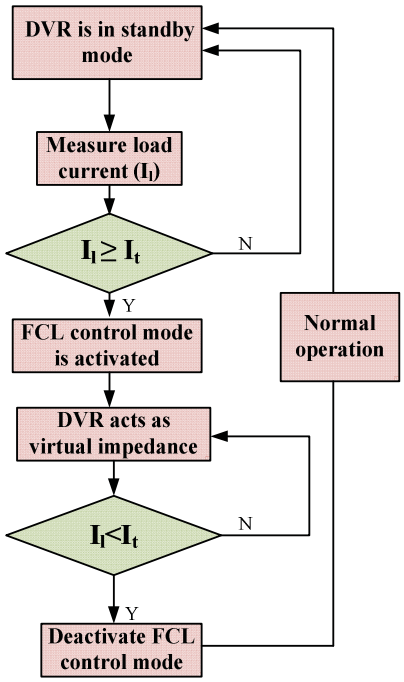

Fig.5 Flow chart for the operation of VI-FCL control algorithm

$$V_{PCC} = \frac{Z_s}{Z_s + Z_l} V_s \tag{2}$$

where Z_s is the source impedance and Z_l is the downstream feeder impedance. From (1) it is clear that the fault currents are very high due to low line impedance which is harmful to the system components and series connected equipment. Similarly, from (2) the PCC voltages will drop which will affect the loads of the other feeders connected to the PCC.

A. *Concept of using DVR as virtual impedance FCL:*

As mentioned earlier the bypass circuit will protect only DVR but PCC voltages are not restored. So in order to reduce fault current the DVR can be controlled to inject voltage in series thus acting like virtual impedance in the line. Consider a downstream fault in the system and let V_{line} be the drop in the nominal line voltage. Fig.2 shows the phasor diagram representation of DVR limiting the fault current. Mathematically the phasor can be represented as follows

$$\vec{\Delta V} = \vec{V}_{inj} + \vec{V}_{Line} \tag{1}$$

$$\vec{\Delta V} = \vec{V}_{inj} + R_{Line}\vec{I}_{Line} + L_{Line}\frac{d\vec{I}_{Line}}{dt} \tag{2}$$

To limit the fault current magnitude at fixed value (say I_t), the phasor V_{line} (i.e., drop across Z_s+Z_l) is controlled in such a way to lie within the dashed circle of radius $I_t\sqrt{(R_s)^2+(\omega L_s)^2}$ as shown in the Fig.2. For the purpose of illustration two possible variations of line voltage phasor on the dashed circle is presented. For these orientations of V_{line} phasor it is possible to draw two DVR injected voltage phasors as shown in the Fig.5a and represented by case:1 and case:2 (V_{inj} and V_{inj}').

By observation it can be inferred that the DVR injection voltage can be minimized by orienting V_{inj} in phase with V_{line} . This implies that for minimal injection the DVR should act as Virtual Impedance whose R/X ratio is proportional to total line impedance during the downstream faults to limit the fault current and also to restore the PCC voltages.

B. *Proposed VI based DFCL control algorithm:*

In [7] flux charge based FCL control algorithm is implemented as active control for DVR, so that it would act as a large virtual inductance in series with the distribution feeder. Upon the occurrence of a downstream fault, the DVR is controlled as a virtual inductor in series with the distribution feeder to limit the fault current and restore the PCC voltage. The main limitations of this method is pure integration of measured voltage may cause saturation of the virtual flux because of the potential DC offset. To demonstrate this phenomenon, the flux-charge based FCL is implemented in PSCAD and the respective results are shown in Fig.3 for three phase fault scenario. During downstream fault (0.5 s to 0.7 s) the rate of change in the line current is more and pure integration of flux results in saturation as shown in Fig.4(a). Due to this the DVR injected voltages are highly distorted as shown in Fig.4. (b) which adverse the situation more. Thus to overcome this situation this paper presents virtual impedance based FCL.

The proposed control scheme is based on virtual impedance concept i.e., by involving additional virtual impedance loops, impedances are introduced into the system during the faults to emulate the physical inductance and resistance in the line. Further, in normal operation, these impedance loops are disabled to avoid unnecessary voltage drop. The Fig.4 shows the proposed control scheme and the flowchart of the operation of proposed FCL scheme is depicted in Fig.5. Firstly, the fault detection block (Fig.4) produces the actuate signals to the impedance loop when an overcurrent (line side) is sensed. Upon the occurrence of downstream fault, the DVR is controlled as virtual impedance in series with distribution feeder line to limit the fault current and restore the PCC voltages. A multiloop control scheme is adopted where the outer loop uses a P+Resonant (PR) controller for voltage control and for inner current loop a proportional controller is employed.

To obtain the inverter output voltage the inverter is modelled by using two terminal equivalent circuit or Thevenin circuit [14] and the respective expression is as follows

$$V(s) = G(s).V_{ref}(s) - Z_{out}(s).I(s) \tag{3}$$

$$Z_{out}(s) = \frac{N(s)(1+K_{ind}M(s))}{1+M(s)N(s)+K_{ind}H_v(s)M(s)N(s)+K_{ind}M(s)} \tag{4}$$

where $M(s) = 1/(L_f s+R_f)$; $N(s) = 1/C_f(s)$; $Z_{out}(s)$ is the output impedance of inverter. The proportional resonant controllers used in the inner voltage control loop is given as

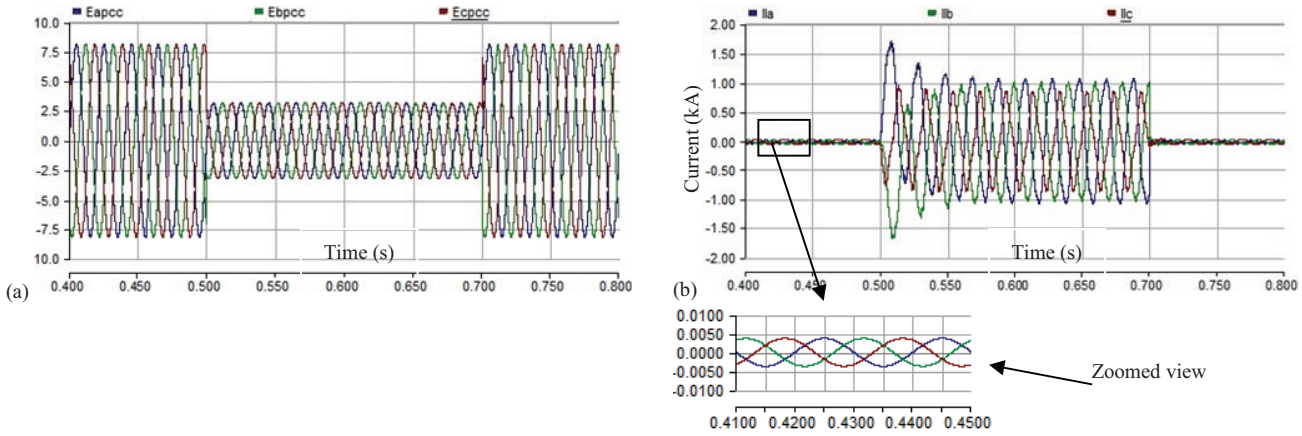

Fig.6 During three-phase short circuit with DVR bypassed: (a) PCC voltages, (b) Line current

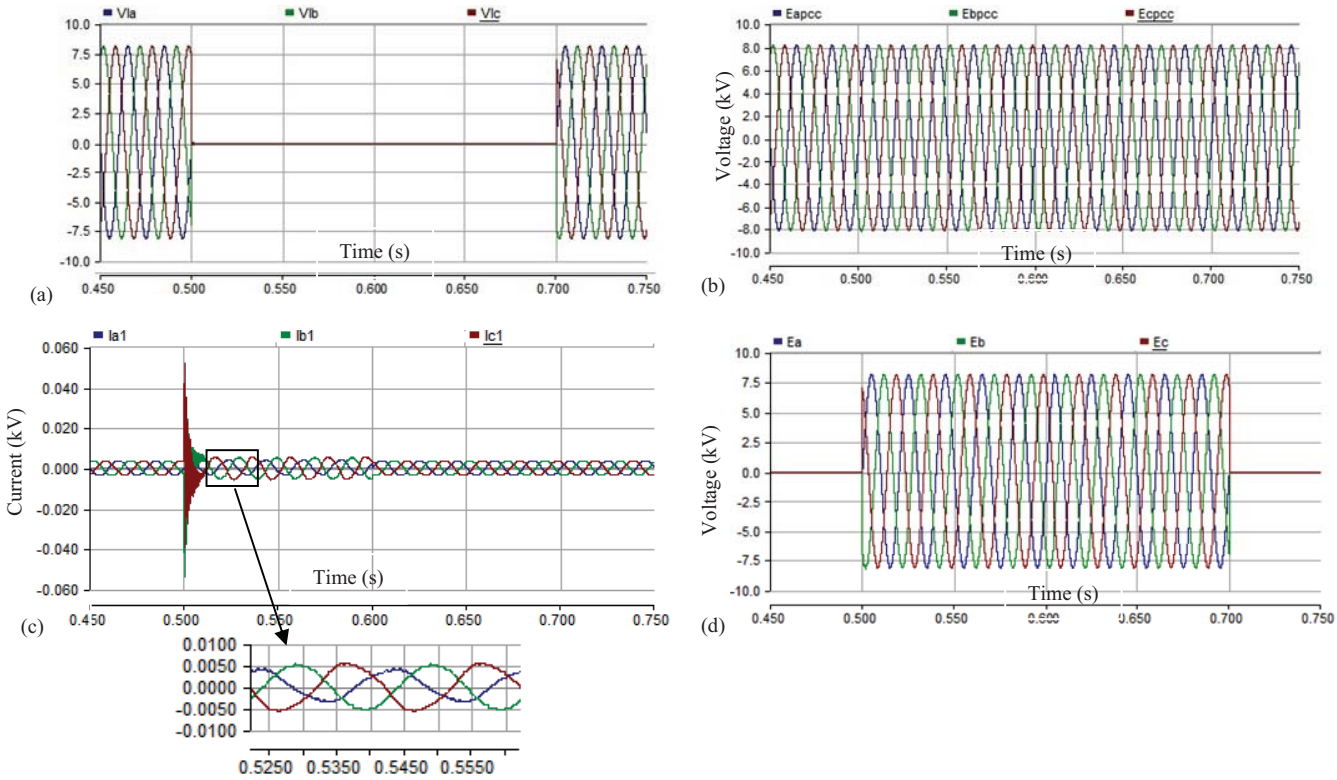

Fig.7 VI based FCL for DVR during three-phase short circuit with (a)Load Voltages, (b)PCC voltages (c) line current, (d) DVR injected voltages

$$G_v(s) = k_{pv} + \frac{k_v s}{s^2 + \omega^2} \quad (5)$$

where k_{pv} and k_v are the gains of proportional and resonant terms in $G_v(s)$. The proportional term k_{pv} is tuned in the similar way as PI controller is tuned and moreover this proportional term particularly in P+R controllers determines the dynamics of the system viz., gain and phase margin and bandwidth [15].The inner current loop controller G_c is a proportional gain controller. The virtual impedance parameter (Z_v) is calculated using the general constraints of transmission line characteristics. A set of constraint equations are formed and iterated by using the MATLAB to fetch the optimum value of Z_v (further detail explanation of design method is given in [12]. By following the method in [12] the optimal value of Z_v obtained is

$$\left|\dot{Z}_v\right| = 1.67\Omega \text{ and } \theta_v = 89^0$$

From the above obtained value of Z_v the respective R_v and L_v values are obtained as ($Z_v \angle \theta_v = R_v + jX_v$) R_v = 24 mΩ and L_v = 0.00139 mH ($X_v = 2\pi f L_v$) .

III. Simulation Results

Simulations using PSCAD/EMTDC have been carried out for a 10-kV system to test the proposed DFCL control algorithm which is based on virtual impedance. The simulations are performed for a symmetrical and asymmetrical downstream

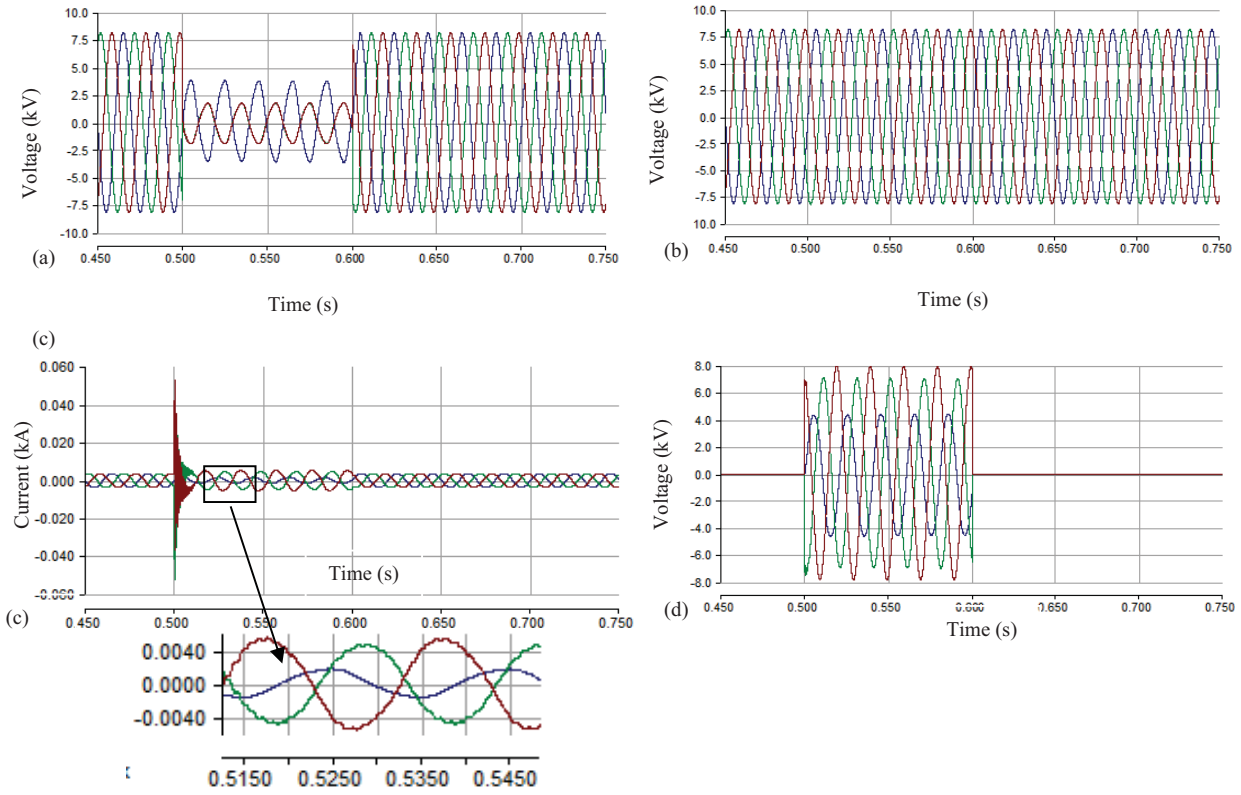

Fig.8 VI based FCL for DVR during two-phase short circuit with (a)Load Voltages, (b)PCC voltages (c) line current, (d) DVR injected voltages

fault. The DVR is connected in series with the distribution feeder and three phases of the load are short-circuited from 0.5 s to 0.7 s.

A. Three phase short circuit fault with DVR in ypass mode

Fig.6(a), (b) show PCC voltages and the line currents respectively, with DVR bypassed. The PCC voltages shown in the Fig.6(a) drop to about more than 50% of the nominal voltage. It is obvious that downstream fault causes extremely high currents (1 kA) compared to nominal value i.e., prefault current (3.6 A) as shown in Fig.6(b) which are due to very low source and line impedance.

B. Three short circuit fault with active control of DVR

The system voltages and currents with DVR actively controlled by proposed DFCL control algorithm which is based on virtual impedance are shown in Fig.9. As expected, the PCC voltages are restored which can be seen from Fig.7(b), by limiting the fault currents (5.2 A as seen from zoomed view). Fig.7 (a),(d) shows the load voltages and DVR injected voltages respectively. Therefore, the loads on other parallel feeders connected to PCC will not be affected.

C. Two phase short circuit fault with active control of DVR

The system is also tested for asymmetrical fault conditions by creating two phase short circuit fault in phase-b and phase-c. Due to the occurrence of the fault the VI-FCL control mode is activated and DVR acts as virtual impedance to limit the fault current. Fig.8(a)-(d) shows the performance of proposed VI based FCL during asymmetrical fault conditions. The fault currents are asymmetrical with slow decay of DC component. As said above during the fault period the currents are limited to 5.2 A from Fig.8(c). From Fig.8(b) it is observed that the PCC voltages are maintained constant even during the asymmetrical fault conditions.

Thus from the above analysis it is concluded that the proposed VI based FCL works efficiently during symmetric and asymmetric faults and to limit the fault current and to restore the PCC voltages.

IV. CONCLUSIONS

In this paper, a DFCL control algorithm based on VI concept is proposed and implemented for DVR to limit the flow of large fault current and restore the PCC voltages and also to protect the DVR during downstream faults conditions. The proposed VI based DFCL act as large virtual impedance in series with distribution feeder. The VI-DFCL is a low cost approach which is implemented without additional equipment. Meanwhile, the simulation studies are carried out for both symmetric and asymmetric faults to test the efficacy of the proposed VI based FCL. The results demonstrate that by using the proposed VI-DFCL the fault currents are limited to 40 A (only1.6 times the rated current) compared to 1 kA when VI-DFCL based control of DVR is bypassed which proves the efficacy of the proposed VI-DFCL control algorithm for DVR.

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