0.5 V, Low Power, 1 MHz Low Pass Filter in 0.18 μm CMOS Process

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Abstract—In this paper a low power continuous-time 4th order low pass Butterworth filter operating at power supply of 0.5 V is presented. A 3-dB bandwidth of 1 MHz using technology node of 0.18 μm is achieved. In order to achieve necessary head-room, the filter uses pseudo-differential bulk-driven transconductor. A master-slave based common mode feedback(CMFB) circuit sets the output common mode voltage of transconductor. The simulation results show that the filter has a dynamic range of 54 dB and consumes a total power of 36 μW when operating at a supply voltage of 0.5 V. The Figure of Merit (FOM) achieved by the filter is 0.05 fJ, lowest among similar low-voltage filters found in the literature. The simulation result show that the 3-dB bandwidth variation for process, voltage and temperature is less than $\pm 10\%$.

Keywords-low-pass filter; continuous-time; bulk-driven; transconductor;

I. INTRODUCTION

The shrinking feature size has always made the circuit designers to look forward to the projected future of semiconductor technology published by International Technology Roadmap for Semiconductors[1]. Continuous technology feature size scaling has enabled denser and faster digital systems. In a typical System On Chip (SOC), analog and RF front end exist along with the digital circuit. The power consumption in digital circuits reduce quadratically with the supply voltage, which has driven the digital industry to move towards low supply voltages. This forced the analog designers to design analog circuits to operate at low voltages. Though the analog design occupies just about 5% to 10% of the total chip area, its functionality is quite important. There is need for more efficient and reliable design approach to be followed in the field of analog circuits to operate at low voltages [2][3]. For low voltage operation, nano-technology devices with low threshold voltage are necessary. However, this requires the designers to move to new technology but at the expense of increased time to market and cost. One way to overcome this problem is to explore the use of existing technology and come up with solutions that make low voltage operation possible and at the same time cost effective. The bulk driven technique is one such solution for low voltage applications [4].

One of the important analog modules on a SOC is a filter performing tasks like anti-aliasing, equalization etc. Filters used in biomedical applications, front end of sensor
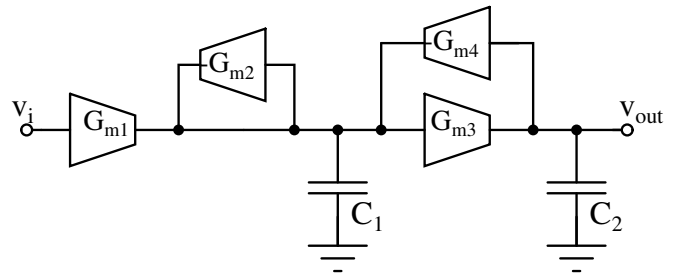

Figure 1. Second order $G_m - C$ filter Architecture

networks demand small size and low power consumption. Therefore there is demand for designing analog circuits that operate at low supply voltages in the range of 1 to 0.5 V with minimum possible power consumption down to the order of few micro watts to few tens of micro watts[5]. [6] proposed an active-RC fifth-order Elliptic 135 kHz low-pass filter that operate at 0.5 V. It is well known fact that for a given power, Transconductor-Capacitor $G_m - C$ filters offer higher bandwidth but at the expense of dynamic range when compared to active-RC filters. The design of $G_m - C$ filter for 0.5 V is, however, not found in literature.

In this paper, a 4th order Butterworth low-pass filter using $G_m - C$ architecture is proposed. The filter is designed to have a 3-dB bandwidth of 1 MHz operating at a power supply of 0.5 V. Two bi-quadratic filter sections are cascaded to realize the 4th order filter.

The rest of the paper is organized as follows. In section II filter implementation details are presented. Section III gives the simulation results and filter performance. Finally conclusions are drawn in section IV.

II. FILTER IMPLEMENTATION

The 4th order Butterworth low-pass $G_m - C$ filter is implemented by cascading two biquadratic filter sections. The schematic of the biquad section shown in Fig.1, where G_m is the transconductance. The pole frequency f_o and the Quality-factor (Q) of the biquad filter is as given in (1) and (2).

$$f_o = \frac{1}{2\pi}\sqrt{\frac{G_{m3}G_{m4}}{C_1 C_2}} \qquad (1)$$
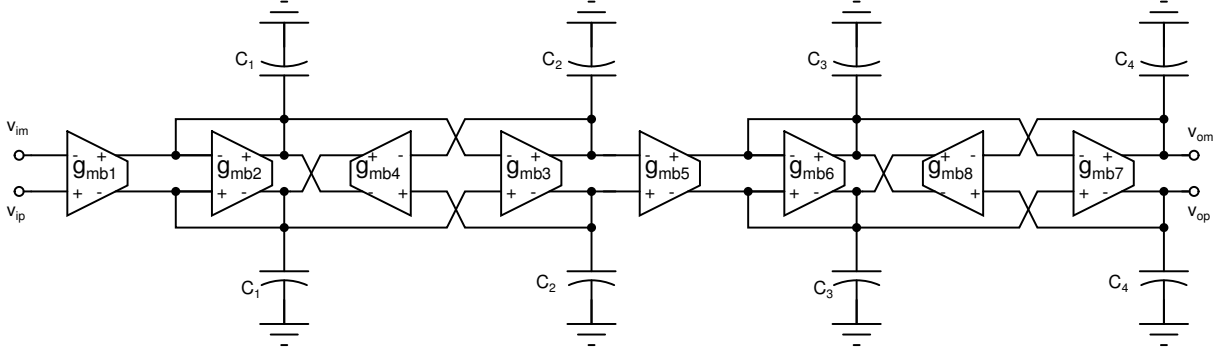
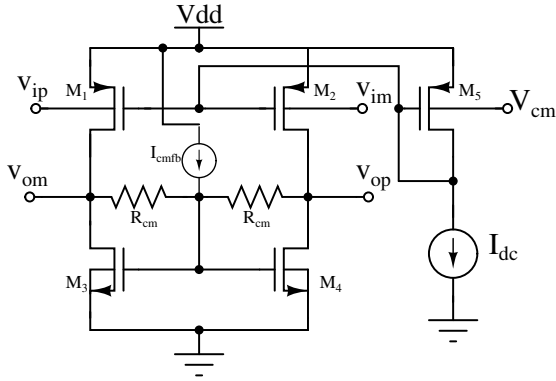Figure 2. Fourth-order fully-differential Gm-C low-pass filter

Figure 3. Schematic of bulk driven pseudo-differential transconductor

and the quality factor is given by

$$Q = \sqrt{\frac{G_{m3}G_{m4}}{G_{m2}^2}}\sqrt{\frac{C_1}{C_2}} \qquad (2)$$

Using the filter table, f_o and Q for each biquad is computed such that the 4th order filter has a 3-dB bandwidth of 1 MHz. In practice, to avoid loss of dynamic range due to possible signal clipping at the output of high-Q sections, the sections are cascaded in the ascending order of Q i.e low-Q section first in the signal path. The fully differential filter realized using two biquads is shown in Fig.2. Note that the transconductors are named g_{mb}'s since the transconductors designed for the filter are bulk driven.

A. Transconductor Design

Transconductor, the building block of the filter, is designed to have bulk-driven inputs and uses pseudo-differential architecture to achieve necessary head-room and signal swing. Fig.3 shows the schematic of the pseudo-differential bulk-driven transconductor used in the present work. v_{ip} and v_{im} are the differential input terminals and v_{op} and v_{om} are the differential output terminals. M_1 and M_2 are PMOS input transistors and M_3 and M_4 form NMOS

current source loads. The input common mode voltage of the transconductor is fixed at 0.25 V and the output common mode voltage is set at 0.25 V by pumping a current I_{cmfb} generated by master CMFB circuit. Each leg of the transconductor is biased with a quiescent current of $2\,\mu$A. The input transistors are sized to have bulk transconductance (g_{mb}) of 10.15 μS.

The response of filter depends on the transconductance and capacitances. The change in the capacitance value over process, voltage and temperature is minimum while transconductance change could be more than 30%. Therefore there is a need for the transconductance to maintain constant across the process, voltage and temperature. The conventional fixed transconductance bias circuits lack the necessary headroom for the satisfactory operation of the loop. In the present work, it is found that the bulk transconductance remains fairly constant with deviation less than $\pm 5\%$ if the current source (I_{dc}) is constant. A constant current generator circuit is designed for the purpose, where an off-chip thermally stable resistor along with negative feedback loop is used. The design of this circuit is not discussed in the present paper.

B. Common mode feedback circuit(CMFB)

Output common-mode voltage of the transconductors is fixed by a master-slave CMFB circuit arrangement. The master CMFB circuit sets the common-mode of a master transconductor using a negative feedback loop and the tuning current is distributed to all filter transconductors. The master CMFB circuit is shown in Fig.4. The common-mode sensing resistor R_{cm}, shown in Fig. 3, is realized by using the transistor M_4 operated in triode region. M_4 is sized to have sufficiently large resistance so that its effect on differential operation (in filter) is minimum. Feedforward capacitor C_{cm} is used in parallel with each R_{cm} to avoid the degradation of the loop phase margin due to the distributed capacitance of resistors. The loop sets the current I_{cmfb} such that the output common-mode voltage ($V_{o,cm}$) is made equal to the reference voltage ($V_{cm,ref}$). The resulting I_{cmfb} is
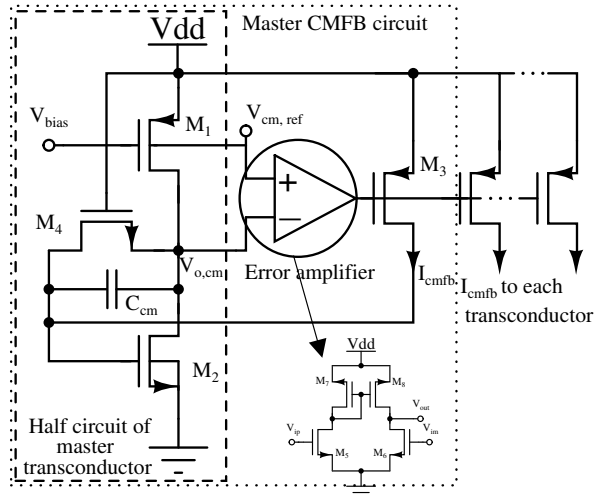
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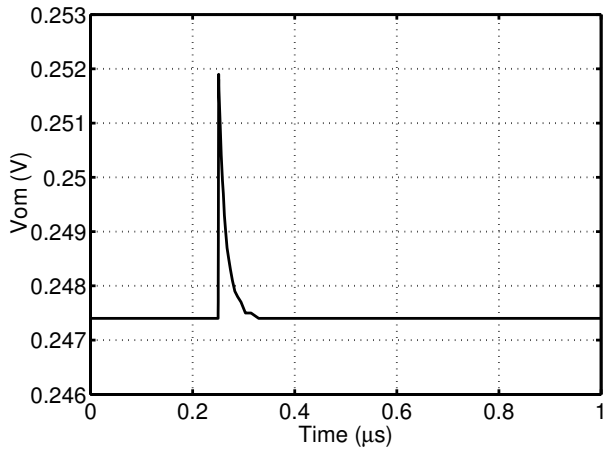Figure 4. Schematic of common mode feedback circuit

Figure 5. Response to common mode current impulse

Figure 6. Magnitude response of Transistor level filter and Ideal filter
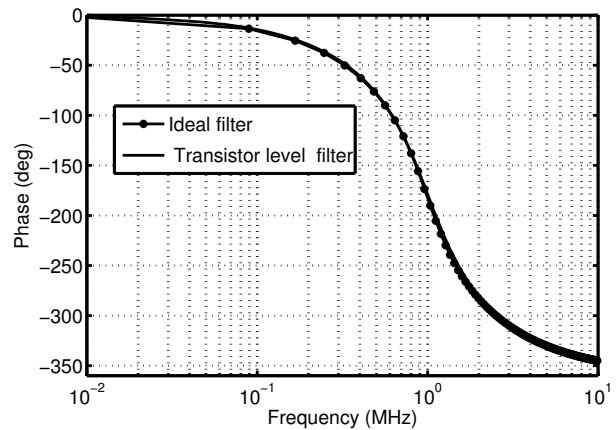
Figure 7. Phase response of Transistor level filter and Ideal filter

distributed to all transconductors using current mirrors. The master CMFB circuit consumes about $3.05\,\mu$W at 0.5 V power supply. The inset in Fig.4 shows the schematic of the error amplifier operating at 0.5 V power supply. The error amplifier is realized using pseudo-differential architecture to overcome the voltage headroom problem. Differential-input single-ended output error amplifier is designed using gate driven NMOS transistors with PMOS current mirror load. The error amplifier designed has a dc gain of 35.55 dB and 3-dB bandwidth of 260 kHz. The Fig.5 shows the stability of the common mode loop for the common mode disturbance.

III. SIMULATION RESULTS

The filter is design centered for non-idealities. The magnitude and phase response of the design centered filter is shown in Fig.6 a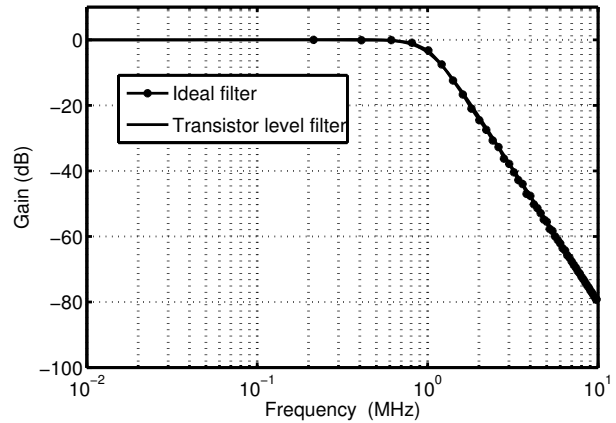nd Fig.7 respectively. The transistor level filter response is compared with the ideal filter and is found to match well with the ideal. The performance parameters of the filter is listed in Table I. The filter consumes $36\,\mu$W while operating at 0.5 V. The power computed include the transconductors, common-mode feedback circuit, a constant current generator circuit (that maintains transconductance across process, voltage and temperature) and bias distribution circuit. The filter offers an input peak-to-peak differential signal swing of 1.2 V at 1% THD for a tone of 330 kHz (one-third of the filter bandwidth). One-third of the filter bandwidth is chosen for the input tone so that the 3rd harmonic, the dominant harmonic, falls on the band-edge of the filter, rather than choosing tone near the band-edge, where the harmonics fall out of the band and gets naturally attenuated due to the filter response.

The performance of the filter is compared with some of the low voltage filters found in the literature and is tabulated in Table II. A figure of merit (FOM) is used for

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Table II
COMPARISON WITH AVAILABLE FILTERS IN LITERATURE

Reference	Bandwidth [MHz]	Order	Supply Voltage [V]	Power [μW]	Q_{max}	Dynamic range@1% THD [dB]	Topology	Technology [μm]	FOM [fJ]
[6]	0.135	5	0.5	1100	6.2	56.6[1]	Active-RC	0.18	0.58
[7]	1.05	3	1.8	4070	1.99	45[2]	Gm-C	0.18	20.53
[8]	0.0175	2	1	45	0.89	63.7[3]	Gm-C	0.35	0.62
[9]	0.010	2	1.5	648	0.707	62.6[3]	Gm-C	0.35	25.18
Present work	1.0	4	0.5	36	0.707	54[4]	Gm-C	0.18	0.05

[1]Ratio of input @100 kHz for 1 % THD to integrated input noise,[2]Ratio of input @1 MHz for 1 % THD to integrated input noise,[3]Ratio of input @1 kHz for 1 % THD to integrated input noise, [4]Ratio of input @330 kHz for 1 % THD to integrated input noise

Table I
PARAMETERS OF 4th ORDER BUTTERWORTH LOW PASS FILTER

Parameters of the filter	Values
Supply [V]	0.5
Technology [μm]	0.18
Cutoff frequency [MHz]	1
Power dissipation [μW]	36
Input [V_{pp}]@ 330 kHz ($f_{o,-3dB}/3$) for 1 % THD	1.2
Dynamic range [dB]	54
Input noise[μV_{rms}]	801

the comparison is computed using (3)[10].

$$FOM = \frac{P_{diss}}{pQ_{max}f_{o}DR^2} \qquad (3)$$

where P_{diss} is the power dissipation, p is the number of filter poles, Q_{max} is the maximum quality factor of the filter poles, f_o is the filter cut-off frequency and DR is the dynamic range. It can be seen that the designed filter has lowest FOM compared to other filters found in the literature that operate at supply voltage ≤ 1 V. A lower FOM indicate more energy efficient design.

It is to be noted that the FOM for the designs given in the Table II are computed from the data available in respective papers.

Simulated output referred noise is shown in Fig.8 and at low frequency it is dominated by 1/f noise. Near the band-edge, thermal nose dominates and it follows the filter response at higher frequency as shown in the inset of Fig.8. The 1/f corner frequency is approximately 200 kHz.

Simulations are run to see the effect of process, supply voltage and temperature on the bulk transconductance. The transconductance variations are shown in Fig.9. The overall transconductance variation due to temperature in the range 0-70°C, for a given corner is found to be less than $\pm 5\%$. The simulation are carried out to observe the effect of process corners, supply voltage and temperature on 3-dB bandwidth of the filter. Fig.10 shows the magnitude response of the designed filter for the typical (tt), slow-slow (ss), fast-fast (ff), slow nmos-fast pmos (snfp) and fast nmos-slow
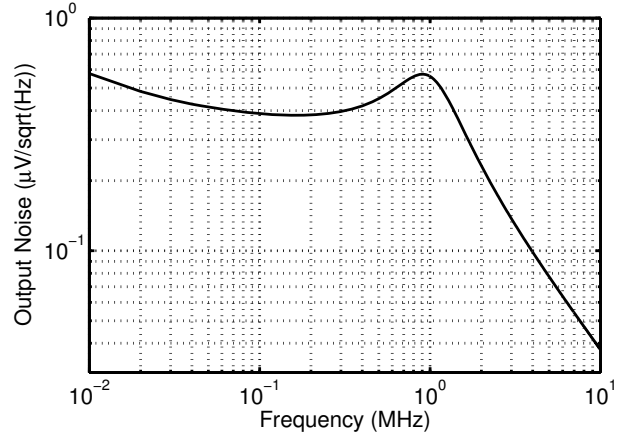

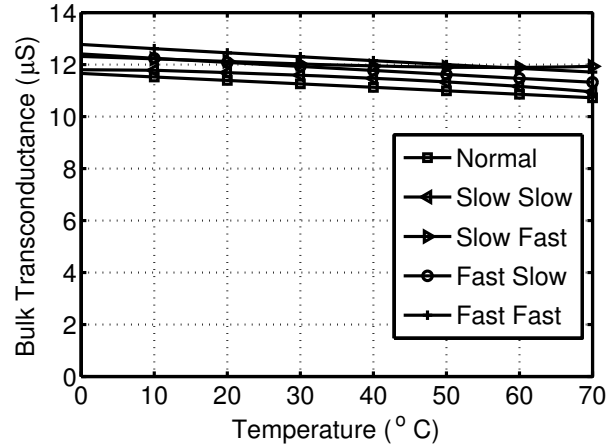Figure 8. Differential output noise of the filter

Figure 9. Transconductance variation with Temperature for different corners

pmos (fnsp) process corners. The observed change in 3-dB bandwidth is $\pm 5.3\%$. Similarly the variation is $\pm 7.5\%$ and $\pm 11\%$ respectively for 10 % change in supply voltage and change in temperature in the range of 0-70°C
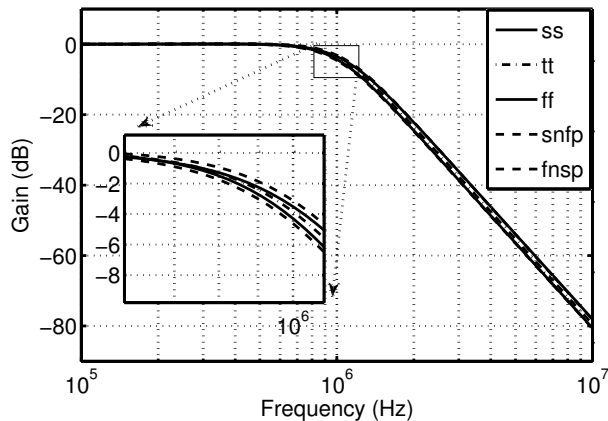
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Figure 10. 3-dB bandwidth variation for different process corners at room temperature

IV. CONCLUSION

A low pass 4th order filter having Butterworth response is designed using $G_m - C$ architecture for a 1 MHz bandwidth, at a supply voltage of 0.5 V in 0.18 μm n-well standard CMOS process. Simulations showed that filter has a dynamic range of 54 dB with power dissipation of 36 μW. The performance of the filter is compared with the filters available in literature. The filter is found to be energy efficient with FOM of 0.05 fJ, an order of magnitude smaller when compared with similar low-voltage designs. Simulated transconductance variations is less than $\pm 5\%$ for a temperature range of 0-70°C and for a given process corners. The 3-dB bandwidth variation for process, voltage and temperature is found to be less than $\pm 10\%$

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