Low voltage current reference circuit with low temperature coefficient

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***Abstract*—Current references are necessary building blocks of every integrated circuit where they are used for biasing analog circuits such as filters, oscillators, phase locked loops, etc. This paper describes the design of a low voltage, low power 10 nA current reference. The proposed current reference circuit is based on a simple design methodology which uses the principle of subtraction of two positive temperature coefficient currents. The circuit is made to operate in sub-threshold region with a supply voltage of 0.5 V. The proposed circuit has been designed and simulated in Cadence Virtuoso with gpdk 180-nm CMOS process. The temperature coefficient of the reference current is 186 ppm/^{o} C over a range from 0 to 80^o C and the variation with supply voltage is 8.02% / V. The total power consumption of the circuit is as low as 45.887 nW.**

***Keywords*—Low-voltage, Low-power, sub-threshold region.**

I. Introduction

Analog and mixed-signal circuits require a stable current reference that is used to set the operating point of the circuits. As the circuit performance varies depending upon the operating point, the current reference should be stable enough to be independent of variations in process, supply voltage and temperature. As the technology is getting scaled down and the demand for portable or battery operated devices is getting increased, it becomes necessary to operate the circuit under low voltages and currents. Another important factor that leads to the reduction in supply voltage is the power consumption. It is found out that dynamic power which includes switching, short-circuit and glitching power is dependent on the supply voltage in quadratic, cubical and quadratic manner respectively and static power has a linear dependence with the supply voltage. So the power consumption can be reduced to a large extent by reducing the supply voltage. As the supply voltage is scaled down, the transistors have to be operated in sub-threshold (weak-inversion) region where gate-to-source voltage of transistor is just below the threshold voltage of the transistor. The bias currents also must be obviously small to satisfy the low power requirements. However, small bias currents (in μA to nA range) are sensitive to temperature variations. A slight change in temperature causes large variation in the current which is not generally acceptable. The threshold voltage of a MOSFET varies negatively with temperature [1]. The mobility also has a negative temperature coefficient as given by the equation (1).

$$\mu(T) = \mu_0(\frac{T}{T_0})^{-m} \tag{1}$$

where T_0 is the room temperature, m has a value between 1.5 and 2 [2]. All these factors, show in turn, the dependence of current with temperature. Hence, there is a need to design robust current reference circuits to overcome the effects of temperature variations.

In [3], Vittoz and Fellrath proposed a current reference operating in the weak inversion region which consists of MOSFETs and a resistor. Later, Oguey [4] made another circuit based on a similar structure by replacing the resistor with a MOSFET. The issue with the above circuits is high temperature coefficient of output currents. Some more similar works have been presented in literature ([5], [6], [7]) which have low temperature coefficient and high accuracy. But most of them cannot be used for low voltage applications as the supply voltage used is high. The paper presented in [8] operates with a low supply voltage, but the temperature coefficient of current is high. In the present paper, a 10 nA current reference circuit with low temperature coefficient and low supply voltage is proposed.

The paper is organized in the following manner. In Section II, design principles of the proposed current reference circuit is explained. Section III describes the proposed current reference circuit. The simulation results and its discussion are presented in Section IV. Conclusions are drawn in Section V.

II. Design principles

Fig. 1 shows the basic current reference circuit [9] using a resistor. As the power supply used in the present work is 0.5 V, all the transistors are made to be operating in sub-threshold region with a bias current in the range of nA.

The equation of drain current in sub-threshold region is given as (2) [5].

$$I_d = I_{d0}\frac{W}{L}e^{\frac{V_{gs}-V_{th}}{\eta V_T}}(1-e^{\frac{-V_{ds}}{V_T}}) \tag{2}$$

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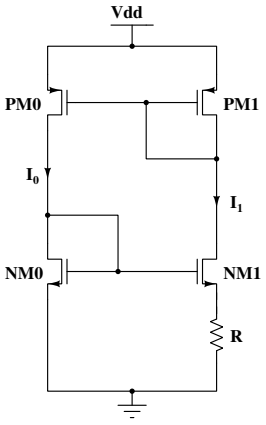

Fig. 1. Basic current reference with resistor

$$I_{d0} = \mu C_{ox}(\eta - 1){V_T}^2$$

where η is the sub-threshold slope factor and its value lies between 1.1 and 1.4, V_T is the thermal voltage which is 25 mV at room temperature. For $V_{ds} > 4V_T$, (2) can be modified to (3).

$$I_d = I_{d0}\frac{W}{L}e^{\frac{V_{gs} - V_{th}}{\eta V_T}} \tag{3}$$

From (3), V_{gs} can be expressed as

$$V_{gs} = \eta V_T ln(\frac{I_d}{I_{d0}(\frac{W}{L})}) + V_{th} \tag{4}$$

In Fig. 1, V_{gs0} (V_{gs} of NM0) can be expressed as in (5).

$$V_{gs0} = V_{gs1} + I_1 * R \tag{5}$$

By substituting (4) in (5),

$$\eta V_T ln(\frac{I_0}{I_{d0}(\frac{W}{L})_0}) + V_{th0} = \eta V_T ln(\frac{I_1}{I_{d0}(\frac{W}{L})_1}) + V_{th1} + I_1 * R \tag{6}$$

Taking the same $\frac{W}{L}$ ratios for transistors PM1 and PM0, I_0 can be made equal to I_1. Applying this to (6), results in,

$$I_1 = \frac{\eta V_T ln(p)}{R} = \frac{\eta KT ln(p)}{qR} \tag{7}$$

where $p = \frac{(\frac{W}{L})_1}{(\frac{W}{L})_0}$ is the ratio of sizes of NM1 and NM0, K is the Boltzmann constant and q is the magnitude of electrical charge.

Differentiating (7) with temperature, we obtain,

$$\frac{\partial I_1}{\partial T} = \frac{\eta K ln(p)}{qR} - \frac{\eta KT ln(p)}{qR^2}\frac{\partial R}{\partial T} \tag{8}$$

Temperature coefficient of $I_1(TC_{I_1})$ is therefore given by (9).

$$TC_{I_1} = \frac{1}{I_1}\frac{\partial I_1}{\partial T} = \frac{1}{T} - \frac{1}{R}\frac{\partial R}{\partial T} \tag{9}$$

The material used for fabrication of resistor is usually polysilicon which has a negative temperature coefficient. So TC_{I_1} will always be positive. This shows that I_1 has a positive temperature dependence.

Using this current reference, a new circuit is proposed which will use another positive temperature coefficient current to nullify the temperature dependence.

III. Proposed current reference circuit

The proposed current reference circuit is shown in Fig. 2. In this circuit, two such above mentioned current references are combined together. As it can be seen from the above figure, the current coming from second circuit is subtracted from the current coming from first circuit and passed through the transistor NM2, which is then mirrored onto NM5 to obtain the resultant reference current (I_{Ref}). Since first circuit is similar to second circuit, the dependency of currents I_1 and I_3 on temperature and supply voltage variations are also similar. As I_{Ref} is obtained by subtracting I_3 from I_1, it is almost independent of temperature and supply voltage variations. The values of I_1 and I_3 can be designed to the required values by adjusting the $\frac{W}{L}$ ratios and the values of resistors. The subtraction is done by mirroring current through transistor PM1 onto PM2 and NM3 onto NM6. The resulting subtracted current is then mirrored onto NM5 to get I_{Ref}.

A start-up circuit is also added in the proposed design. As this is a self-biased circuit, there is a possibility that the circuit will be driven to an unwanted operating point which results in zero current. This occurs when the gates of the transistors NM0 and NM1 are at ground and gates of PM0 and PM1 are at V_{dd}. Hence, no current flows in the circuit and the circuit fails to give the desired output. The gate voltage of NM8 is somewhere in between V_{dd} and $V_{dd} - V_{thp}$. Therefore, NM8 turns on and it leaks the current from the gates of PM0 and PM1 to the gates of NM0 and NM1. So, the voltage at the gates of NM0 and NM1 rises and the circuit goes into the desired state. When the gate voltage of NM0 / NM1 rises, NM7 turns on and reduces the gate voltage of NM8. This will turns off NM8 and the start-up circuit is disconnected from the main circuit. Similar operation happens in the right half of the circuit.

IV. Simulation results and comparison

The proposed current reference circuit has been designed and simulated in Cadence Virtuoso with gpdk 180-nm process. The circuit generates a reference current of 10 nA.

Fig. 3 illustrates the working principle of the proposed circuit. As shown in figure, I_2 and I_6 have positive temperature

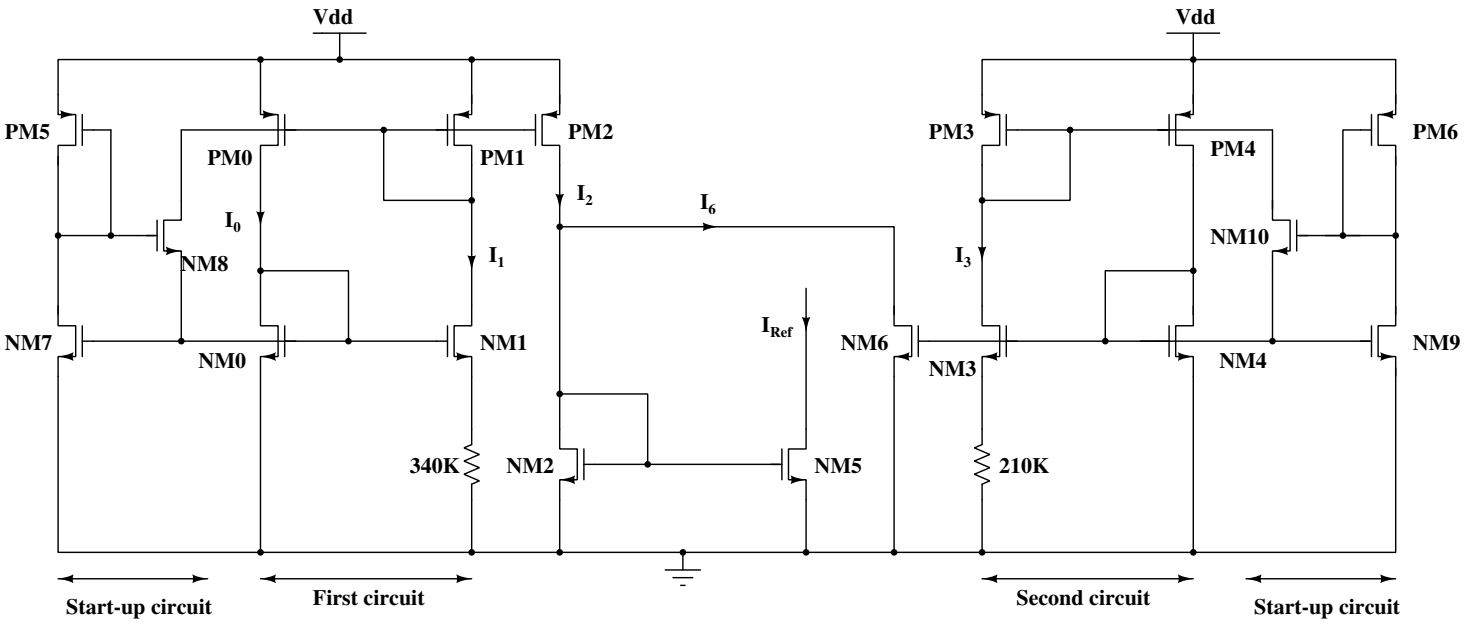

Fig. 2. Proposed current reference

coefficient. I_{Ref} has a value that is equal to the difference of I_2 and I_6.

Simulations are carried out to observe the effect of temperature and supply voltage variations on I_{Ref}. In Fig. 4, I_{Ref} is plotted against the temperature in the range of 0 to 80^o C. The temperature coefficient of $I_{Ref}(TC_{I_{Ref}})$ is found to be as low as 186 ppm/^{o} C for a supply voltage of 0.5 V.

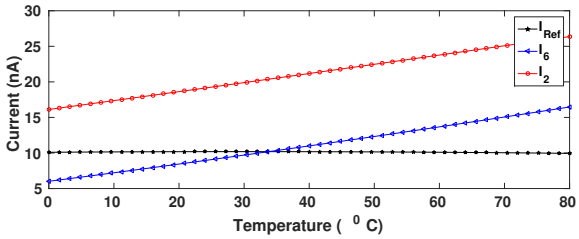

Fig. 3. Illustration of working principle

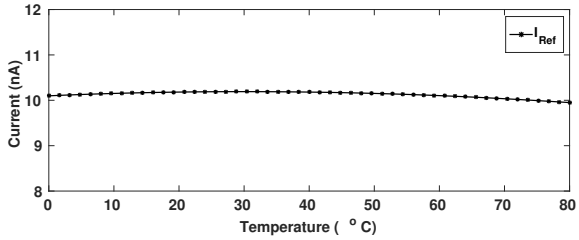

Fig. 4. Plot of current vs. temperature

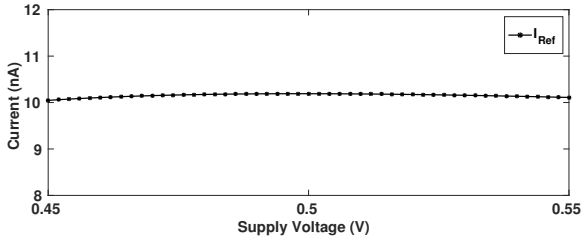

Fig. 5. Plot of current vs. supply voltage

Figure 5 shows reference current versus supply voltage plot. The supply voltage is varied from 450 mV to 550 mV ($\pm$ 10 %). The variation in I_{Ref} with supply voltage is found to be 8.02 %/ V at room temperature. Total power consumption of the circuit is 45.887 nW.

A performance comparison of the proposed current reference circuit with other similar works found in the literature is given in Table 1. It can be seen that, the proposed circuit operates with lowest supply voltage. The performance in terms of temperature coefficient is better compared to all the papers listed. Hence, the proposed circuit can be used as an efficient current reference circuit in low voltage, low power analog circuits.

TABLE I
COMPARISON WITH OTHER DESIGNS

Parameters	[6]	[8]	[10]	[5]	**This work**
Technology(μm)	3	0.18	0.8	2	**0.18**
Reference current (nA)	774	26.1	430	287	**10**
Supply voltage (V)	3.5	1	2.5	–	**0.5**
Supply current (nA)	2000	52	860	–	**91.77**
TC (ppm/^oC)	375	202.1	600	226	**186**

V. Conclusion

In this paper, a low voltage 10 nA current reference has been presented with a supply voltage of 0.5 V in 180-nm CMOS technology. Simulation results show a temperature coefficient as low as 186 ppm/^{o} C, a supply voltage sensitivity of 8.02 %/ V and a power consumption of 45.887 nW. The proposed circuit can be used as an efficient current generator for low voltage, low current analog circuits.

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