Performance Analysis of PWM Strategies for Cascaded H-Bridge Three-Level Inverter

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***Abstract*- Multilevel inverters with various pulse width modulation strategies have established their importance in high power high performance industrial applications, as they can synthesize output waveform with improved harmonic spectrum. This paper presents the performance analysis and comparison of different PWM strategies for cascaded H-bridge three-level inverter in terms of line voltage and motor current *THD* with their fundamental components. It is shown that harmonic loss minimized optimal-SHEPWM strategy gives better results in terms of voltage *THD* compared to SPWM, SVPWM and SHEPWM strategies.**

***Index Terms*- Harmonic distortion, Pulse width modulation, Pulse width modulated inverters, Three-Level inverter.**

I. INTRODUCTION

In high performance, high power and medium voltage induction motor drive applications the three-level (Pulse Width Modulation) PWM Inverters has drawn very much interest in industry. As they have many benefits such as sophisticated PWM strategies, reduced energy consumption, and the elimination of lower order voltage harmonics. In three-level inverter the total harmonic distortion (*THD*) is low and also less voltage stress on switching devices compared to two- level inverter [1-6]. The most common three-level inverter topologies are the diode-clamped or neutral point-clamped (NPC), capacitor-clamped or flying capacitor-clamped and the cascaded H-bridge inverter [1]. In this paper the cascaded H-bridge inverter as shown in fig.1 is considered for analysis. The cascaded inverter uses series connection of single-phase full bridge inverter called H-bridge cell to construct multilevel inverter with separate dc source. Each single-phase full-bridge inverter generates three voltage levels at the output $+V_{dc}$, 0, and $-V_{dc}$ as shown in Table. I. The main features of this topology are the modular structure results in high reliability, requires least number of devices to realize multilevel inverter [1-4]. Each cell requires separate dc source, hence a multiple winding transformer is required at the input stage. This will add to system cost but improves the input waveforms. The performance of a three-level inverter depends on the type of pulse width modulation strategy used. In the literature various PWM strategies [20] have been reported and only sine-triangle PWM (SPWM) [8-10], harmonic loss minimized optimal-SHEPWM (HLM-SHEPWM) [25], selected harmonic elimination PWM (SHEPWM) [16-22] and space vector PWM (SVPWM) [11-12,14-15] are presented in this paper.

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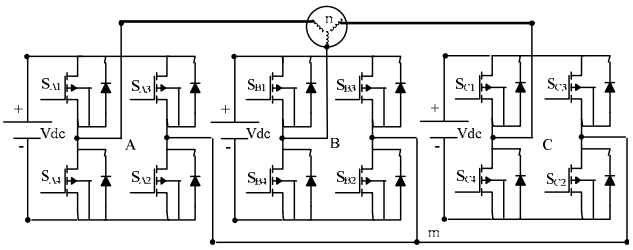


Fig. 1. Three-level cascaded H-bridge inverter topology

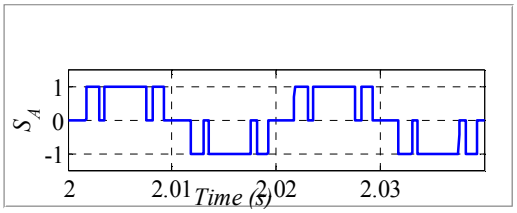
The PWM strategies for three-level inverter are explained in section II. Simulation results and performance analysis are presented in section III. The performance is studied in terms of *THD* and magnitude of fundamental voltage of the line voltage. The outlines are concluded in section IV.

TABLE I
SWITCHING STATUS AND VOLTAGE LEVEL OF THREE-LEVEL CASCADED H-BRIDGE INVERTER

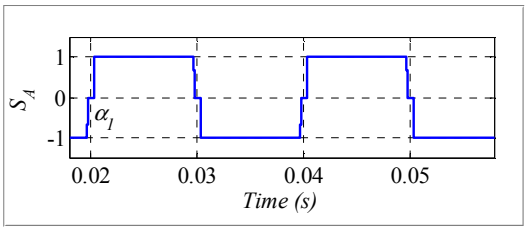
Switches	Switching state	Voltage level
S_{A1}, S_{A2}	ON	$+V_{dc}$
S_{A3}, S_{A4}	ON	$-V_{dc}$
S_{A1}, S_{A3} *or* S_{A4}, S_{A2}	ON	+0 or -0

II. PWM STRATEGIES FOR THREE-LEVEL INVERTER

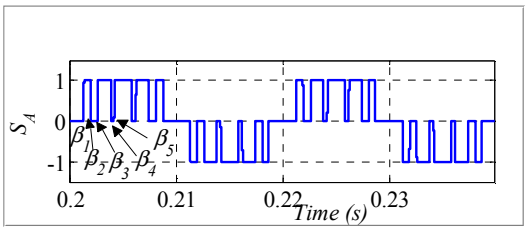
Based on switching frequency of the multilevel inverter PWM strategies can be classified into various schemes [1, 20]. In this paper we have considered SPWM, HLM-SHEPWM, SHEPWM and SVPWM for performance analysis. A very popular method in industrial applications is the triangular (carrier) based SPWM that uses the phase shifting technique to reduce the harmonics in the output voltage. The sinusoidal PWM is easy to implement in hardware by analog as well as digital controllers. However, due to the variation of the values of the reference wave during a PWM period, the relation between the reference wave and carrier wave is not fixed and results in loss of synchronization between reference and carrier wave and hence loss of symmetry as well. As a result of this sub harmonics may introduce in the output voltage due to which the speed of the motor may suffer from low frequency pulsations. SVPWM is a space vector control based PWM strategy that gives lower *THD* with higher voltage. The hardware implementation of this strategy is simple and can be done either by using digital signal processor (DSP) or by using Field Programmable Gate Arrays (FPGA) based controllers. Also SVPWM symmetrically splits dwell time of the zero vector which helps in reducing the THD [11, 12]. These features make it suitable for high-voltage high power



(a)



(b)



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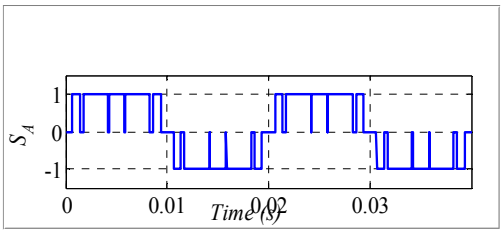

(d)

Fig. 2. Switching pulses of phase A (a) SPWM (b) HLM-SHEPWM (c) SHEPWM (d) SVPWM

applications. In SVPWM, instead of using a separate modulator for each of the three phases, the three phase quantities are transformed to equivalent two phase quantity either in stationary reference or synchronously rotating frame. It has been shown, that SVPWM generates less harmonic distortion in both output voltage and current applied to the phases of an induction motor and provides a more efficient use of the dc bus in comparison with SPWM strategy. The switching pulses for SPWM and SVPWM are shown in Fig. 2 (a) and (d) respectively. In HLM-SHEPWM and SHEPWM strategies the basic idea is to minimize harmonic distortion by removing the desired harmonics presenting in the waveform and to achieve variable amplitude of the fundamental component. But usually the lower order harmonics (all odd lower order harmonics in case of single phase and all odd non triplen lower order harmonics in the case of three phase) are chosen for elimination by properly selecting the switching angles of multilevel inverters. The number of harmonics elimination depends on the number of chopping per quarter-cycle. If there are C chopping per quarter-cycle then (C-1) odd harmonics can be eliminated [16]. The switching angles for HLM-SHEPWM and SHEPWM as shown in Fig. 3 (α_1=5.2538^0) and Fig. 4 (β_1=23.5835^{0,} β_2= 32.6015^{0,} β_3= 45.6433^{0,} β_4=68.4980^{0,} β_5= 76.0978^0) respectively are calculated using Newton-Raphson method for five iterations with initial switching angles are assumed as α_1=5^0 for HLM-SHEPWM and β_1=23^{0,} β_2= 32^{0,} β_3= 45^{0,} β_4= 68^{0,} β_5= 76^0 for SHEPWM. In order to keep the number of harmonics which are eliminated at a constant level the switching angle of these strategies must be less than $\pi/2$. In spite of that, these schemes are invalid if the switching angles are not less than $\pi/2$.

III. Simulation Results and Performance Analysis

PWM strategies for three-level inverter are simulated using MATLAB/SIMULINK with solver ode45 (Dormand-Prince) of variable-step type, relative tolerance of 1e-3 and applied to a *v/f* drive consists of a 440V, 3.75KW, 1450rpm, three phase rpm induction motor powered from a three level IGBT based inverter. The results of line voltage and motor current *THD* along with the fundamental components are tabulated in Table II for different PWM strategies. The switching pulses for phase A is shown from Fig. 2 (a) to (d) for SPWM, HLM-SHEPWM, SHEPWM and SVPWM respectively for two cycles.

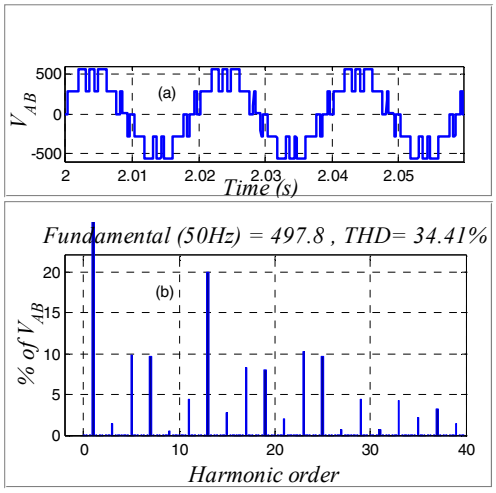

Fig. 3. Waveform of (a) Line voltage V_{AB} (b) Harmonic spectrum of SPWM

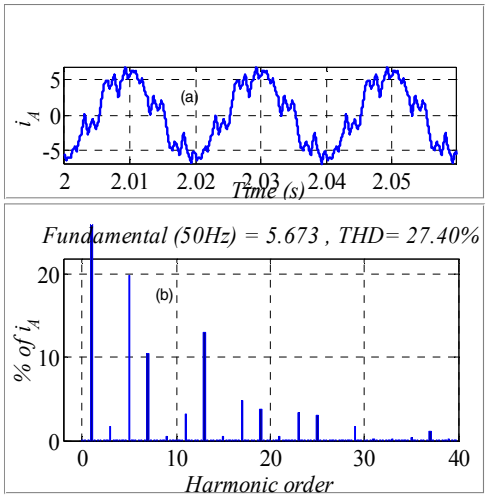

Fig. 4. Waveform of (a) Motor current i_A (b) Harmonic spectrum for SPWM

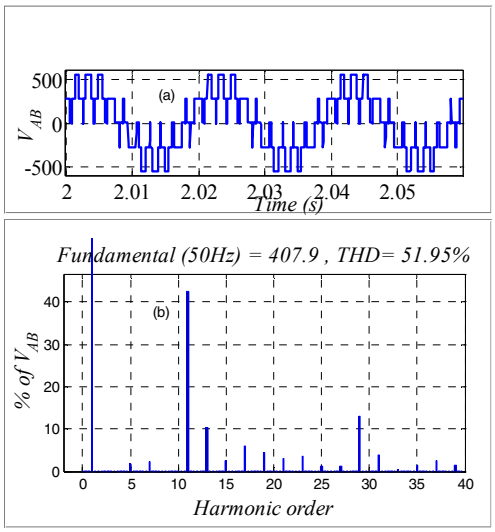

Fig. 5. Waveform of (a) Line voltage V_{AB} (b) Harmonic spectrum of SHEPWM

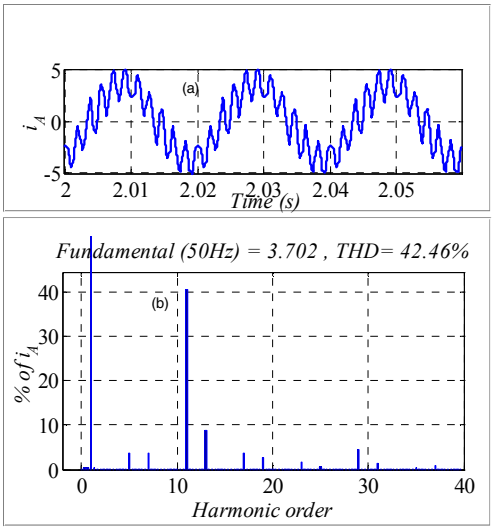

Fig. 6. Waveform of (a) Motor current i_A (b) Harmonic spectrum for SHEPWM

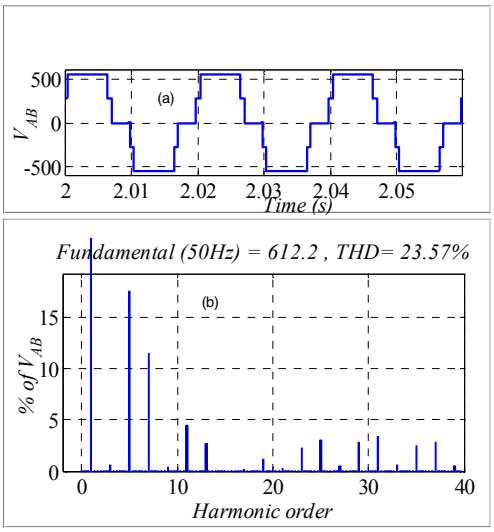

Fig. 7. Waveform of (a) Line voltage V_{AB} (b) Harmonic spectrum for HLM-SHEPWM

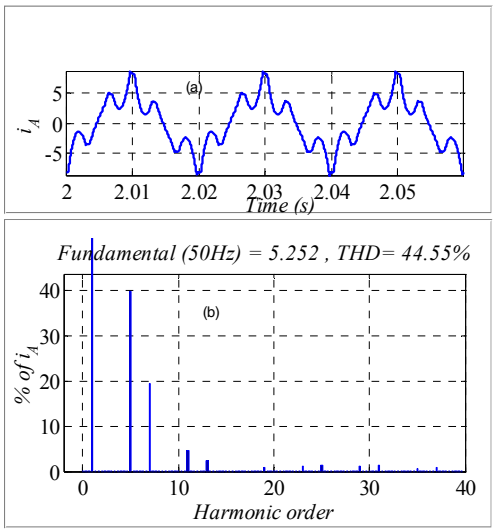

Fig. 8. Waveform of (a) Motor current i_A (b) Harmonic spectrum for HLM-SHEPWM

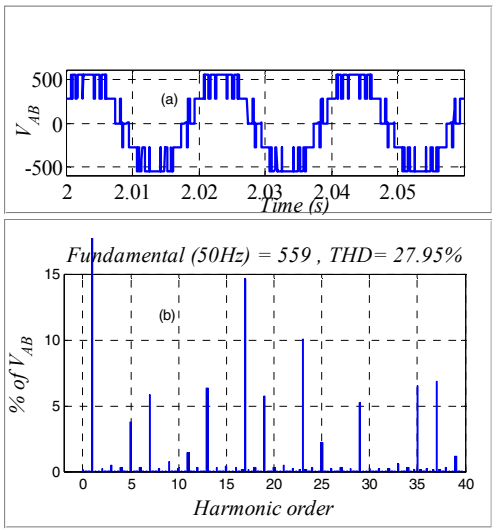

Fig. 9. Waveform of (a) Line voltage V_{AB} (b) Harmonic spectrum for SVPWM

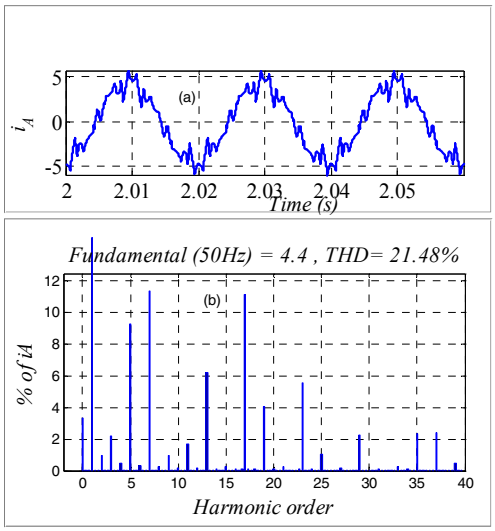

Fig. 10. Waveform of (a) Motor current i_A (b) Harmonic spectrum for SVPWM

TABLE II
THD AND FUNDAMENTAL COMPONENT OF LINE VOLTAGE AND MOTOR CURRENT FOR DIFFERENT PWM STRATEGIES

PWM Strategies	V_{AB} fundamental	*THD of* V_{AB} (%)	i_A fundamental	*THD* of i_A (%)
SPWM	497.8	34.41	5.673	27.40
HLM-SHEPWM	612.2	23.57	5.252	44.55
SHEPWM	407.9	51.95	3.702	42.46
SVPWM	559	27.95	4.4	21.48

The harmonic plots are plotted and *THD* are calculated using integral cycle data for both line voltage and motor current.

IV. CONCLUSIONS

In this paper the performance of various PWM strategies in terms of line voltage and motor current *THD* along with their fundamental components are studied and compared. The simulation results for different strategies with their harmonic spectrums are presented. In all these cases, symmetry and synchronization, is maintained. This is essential for high power low switching frequency applications. From the results, it can be shown that the HLM-SHEPWM strategy gives improved results for line voltage but it gives poor motor current *THD* compared to other PWM strategies. The reason for poor motor current *THD* is that HLM-SHEPWM does not guarantee the elimination of lower order harmonics and it only results in optimal harmonic loss. SVPWM strategy is a better choice in terms of motor current *THD* but gives lesser line voltage and slightly higher line *THD* than HLM-SHEPWM. Also SVPWM gives better performance than SPWM and SHEPWM strategies.

REFERENCES

[1] J. Rodriduez, J.S. Lai, F.Z.Peng "Multilevel Inverters: A Survey of Topologies, Controls and Applications" *IEEE Trans. On IE*, vol.49, No.4, pp.724-738, August 2002.

[2] B.P. McGrath, D.G. Holmes "Multicarrier PWM Stategies for Multilevel Inverters" *IEEE Trans. On IE*, vol.49. No.4, pp.858-867, August 2002.

[3] N. S. Choi, J. G. Cho, G. H. Cho, "A General Circuit Topology of Multilevel Inverter," *Proc. IEEE PESC'91*, pp. 96–103. 1991.

[4] B. Velaerts, P. Mathys, "New developments of 3-level PWM strategies," in *Proc. EPEC*, Aachen, Germany, 1989, pp. 411–416.

[5] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, G. Sciutto, "A new multilevel PWM method: A theoretical analysis," *IEEE Trans. Power Electron*., vol. 7, pp. 497–505, July 1993.

[6] C. Rech, H. Pinheiro, H.A. Grundling, H.L. Hey, J.R. Pinheiro "Analysis and Comaprision of Hybrid Multilevel Voltage Source Inverters" *IEEE 32rd Annual Power Electronics Specialists Conference*, vol.2, pp.491-496, 2002.

[7] H. L. Liu and G. H. Cho, "Three level space vector PWM in low index modulation region avoiding narrow pulse problem," IEEE Trans. Power Electron., vol. 8, pp. 481–486, Sept. 1994.

[8] F.Wang "Sine-Triangle versus Space-Vector Modulation for Three-Level PWM Voltage-Source Inverters" IEEE Trans. On IA, vol.38, No.2, pp.500-506, March/April 2002.

[9] D.G. Holmes, B.P. McGrath, "Opportunities for harmonic cancellation with carrier based PWM for two-level and multi-level cascaded inverters," *IEEE Trans. Ind. Applicat.,* vol. 37, pp. 574–582, March-April 2001.

[10] S.R. Bowes, "New sinusoidal pulse-width modulated inverter," *Proc. Inst. Elect. Eng.*, vol.122, No.11, pp.1279–1285, November. 1975.

[11] G. Narayanan, V. T. Ranganathan, "Synchronized PWM strategies based on space vector approach. Part 1: Principle of waveform generation," IEE Proc-Electr. Power Appl., vol. 146, No. 3, pp. 267-275, May 1999.

[12] A. R. Beig, G. Narayanan, and V. T. Ranganathan, "Modified SVPWM Algorithm for Three Level VSI with Synchronized and Symmetrical Waveforms," IEEE Transactions on Industrial Electronics, vol. 54, pp. 486–494, February 2007.

[13] C.Cecati, A. Dell'Aquila, A. Lecci, M. Liserre, V.G. Monopoli, "A discontinuous carrier-based multilevel modulation for multilevel converters," 3^{0th} Annual Conference of IEEE Industrial Electronics Society, IECON 2004, vol1, pp 280-285, 2004.

[14] A. K. Gupta, A. M. Kambadkone, "A General Space Vector PWM Algorithm for Multi-level Inverters, Including Operation in Overmodulation range" IEEE Trans. PE, vol. 22, no. 2, pp. 517-526, 2007.

[15] J. T. Boys and P. G. Handley, "Harmonic analysis of space vector modulated PWM waveforms," Proc. Inst. Elect. Eng., pt. B, vol. 137, no. 4, pp. 197–204, July 1990.

[16] J.R. Espinoza, G. Joos, J.I. Guzman, L.A. Moran, R.P. Burgos "Selective Harmonic Elimination and Current/Voltage Control in Current/Voltage-Source Topologies: A Unified Approach" *IEEE Trans. On IE*, vol. 48. No.1, pp.71-81, February 2001.

[17] T. Tang, J. Han, X. Tan "Selective Harmonic Elimination for a Cascade Multilevel Inverter" *IEEE-ISIE*, pp.977-981, July 2006.

[18] J. Kumar, B. Das, P. Agarwal "Selective Harmonic Elimination Technique for a Multilevel Inverter" *Fifteenth National Power Systems Conference (NPSC), IIT Bombay,* pp.608-613, Dec 2008.

[19] V.G. Agelidis, A.I. Balouktsis, C. Cossar "On Attaining the Multiple Solutions of Selective Harmonic Elimination PWM Three-Level Waveforms Through Function Minimization" *IEEE Trans. On IE*, vol.55, No.3, pp.996-1004, March 2008.

[20] L. Li, D. Czarkowski, Y. Liu, P. Pillay "Multilevel Selective Harmonic Elimination PWM Technique in Series-Connected Voltage Inverters" *IEEE Trans. On IA*, vol.36, No.1, pp.160-170, Jan/Feb 2000.

[21] D. Ahmadi, J. Wang "Selective Harmonic Elimination for Multilevel Inverters with Unbalanced DC Inputs" *IEEE Vehicle Power and Propulsion Conference*, pp.773-778, 2009.

[22] P.N. Enjeti, P.D. Ziogas, J.F. Lindsay, "Programmed PWM techniques to eliminate harmonics: A critical evaluation," *IEEE Trans. Ind.Appl.*, vol. 26, No. 2, pp. 302–316, Mar./Apr. 1990.

[23] S. Barkati, L. Baghli, E.M. Berkouk, M.S. Boucherit "Harmonic Elimination in Diode-Clamped Multilevel Inverter using Evolutionary Algorithms" *Electric Power Systems Research, Elsevier*, pp.1736-1746, May 2008.

[24] A.I. Maswood, L.Jian "Optimal Online Algorithm Derivation for PWM-SHE Switching" *IEE Electronis Letter, online No. 19980578*. Vol.34, No.8, pp. 821-823, April 1998.

[25] S.Halasz "Optimal Control of Three-Level PWM Inverters" IEEE Trans. On IE, vol.44, No.1, pp.96-106, February 1997.