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A 0.3 V, 56 dB DR, 100 Hz fourth order low-pass filter for ECG acquisition system

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ABSTRACT

This paper proposes an extremely low voltage, low power bulk-driven voltage follower (BD-VF). As an application of the proposed BD-VF, a 4th order low-pass filter (LPF) with cutoff frequency adjustable from 50 Hz to 250 Hz is designed for electrocardiogram (ECG) acquisition systems. The filter is implemented in UMC 180 nm CMOS technology occupying only 0.03 mm^2 area. Post layout simulation results show that the filter offers 56 dB dynamic range even with an extremely low supply voltage of 0.3 V. The total power consumption of the filter is 4.8 nW for a cutoff frequency of 100 Hz. The Figure-of-merit (FoM) and capacitance/pole of the filter are 5.7×10^{-15} and 2.2 pF respectively. The proposed filter offers the lowest FoM compared to the state-of-the-art nW-class filters.

1. Introduction

The rapid growth of battery operated implantable and portable medical devices necessitate extremely low voltage and low power integrated circuits to increase the battery life. Low-pass filter (LPF) is an important building block in front-end processing of electrocardiogram (ECG) signal. A typical data acquisition system for the processing of ECG signal is shown in Fig. 1 [1]. The pre-amplifier amplifies the weak ECG signal (100 μV - 4 mV) and the LPF increases frequency selectivity by eliminating out-of-band noise. Finally, analog-to-digital converter (ADC) converts the analog signal into digital signal. The highest frequency component in an ECG can lie anywhere between 100 Hz and 250 Hz [2] and hence the cutoff frequency of the LPF used in the processing of these signals also must be in the same range. Large capacitors and large resistors are required to design the LPF with such large time constant (low cutoff frequency), resulting in area overhead. Hence, the major challenges in the design of these filters are low voltage, less area and low power consumption.

For low frequency applications, most of the filters reported in the literature are of $G_m - C$ (Transconductor-Capacitor) topology, in which the cutoff frequency is determined by $G_m/2\pi C$. In this case, either large C or low G_m is required to get low cutoff frequencies. Capacitance value can be increased by using capacitance multiplier circuits

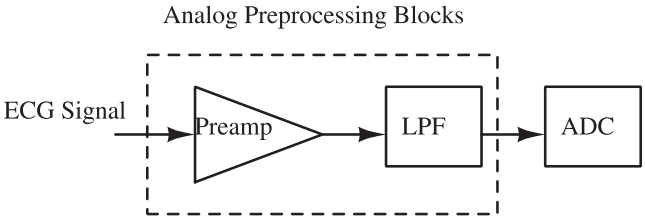

Fig. 1. ECG acquisition system.

[3–5]. However, these circuits consume extra power and produce extra noise. On other hand, there are G_m reduction techniques [3,6–8], such as current division, current cancellation. However these techniques demand large power. In general, bulk transconductance (g_{mb}) [9] is less than gate transconductance (g_m) and hence bulk-driven transconductors [7,10,11] are widely used to design LPFs with low cutoff frequency.

Many single branch filters, such as source follower (SF) and voltage follower (VF) based filters are reported in Refs. [12,13] for low frequency applications. The internal negative feedback available in SF

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and VF filters makes them more linear compared to simple $G_m - C$ filters. In Ref. [14], a 4th order band-pass filter is realized by cascading SF bi-quads. In a similar fashion, 4th order LPFs using flipped VFs for ECG signal processing are reported in Refs. [15,16]. A 4th order, sub-threshold buffer based LPF is presented in Ref. [17]. All these filter designs reported in literature are implemented with a supply voltage of 0.5 V or higher.

The main objective of this paper is to design an LPF with ultra low supply voltage, low power for ECG signal processing. A simple bulk-driven voltage follower (BD-VF), which operates with a supply voltage of 0.3 V, is proposed. This proposed BD-VF is used to design a 4th order LPF with cutoff frequency adjustable from 50 Hz to 250 Hz. In Section 2, the design of proposed BD-VF and 4th order LPF are discussed. Section 3 discusses the post-layout simulation results and the paper is concluded with Section 4.

2. Proposed BD-VF

Bulk-driven transistors offer more signal swing even under low supply voltage conditions [18]. The ratio g_{mb}/g_m is typically 0.2–0.4 [7]. Because of its smaller transconductance and suitability for low voltage operations, bulk-driven topology is used in this design. In sub-threshold region, the expression for g_{mb} is given by (1) [19].

$$g_{mb} = (\eta - 1)g_m = (\eta - 1)\frac{I_o}{\eta V_T} \tag{1}$$

where I_o is the current flowing through the transistor, η is the sub-threshold slope factor and V_T is the thermal voltage.

The proposed BD-VF is shown in Fig. 2(a). All the transistors are operating in weak-inversion saturation region ($V_{GS} < V_{th}$ and $V_{DS} \geq 3V_T$). The input signal is applied to the bulk terminal of M_1. The bulk, drain terminals of M_2 and drain of M_1 are shorted together. Transistor M_2 (with bulk connected to drain terminal) makes the gain of the circuit approximately equal to unity as explained later in this Section. An integrating capacitor (C) is connected at the output node, which makes the circuit a first order LPF.

Fig. 2(b) shows the small signal equivalent of the proposed BD-VF. Here, $r_x = r_{o1} \parallel r_{o2} \parallel r_{o3}$. All the terms have their usual meanings. The expression for the transfer function can be derived as follows. By applying KCL at node D_1,

$$g_{m1}v_{gs1} + g_{mb1}v_{bs1} + v_o(g_{mb2} + \frac{1}{r_x} + Cs) = 0 \tag{2}$$

By substituting $v_{gs1} = 0$, $v_{bs1} = v_{in}$ in (2) and simplifying, we get the transfer function, $H(s)$.

$$H(s) = -\frac{\frac{g_{mb1}r_x}{1+g_{mb2}r_x}}{1 + \frac{r_x}{1+g_{mb2}r_x}Cs} \tag{3}$$

From (3), the DC gain (A_o) and the time constant (τ) can be expressed as

$$A_o = -\frac{g_{mb1}r_x}{1 + g_{mb2}r_x} \tag{4}$$

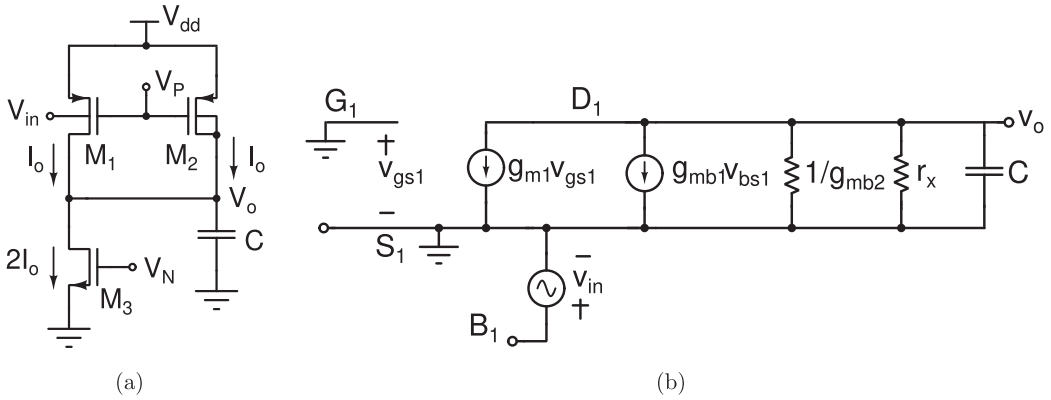


Fig. 2. (a) Proposed BD-VF, (b) Small signal equivalent circuit.

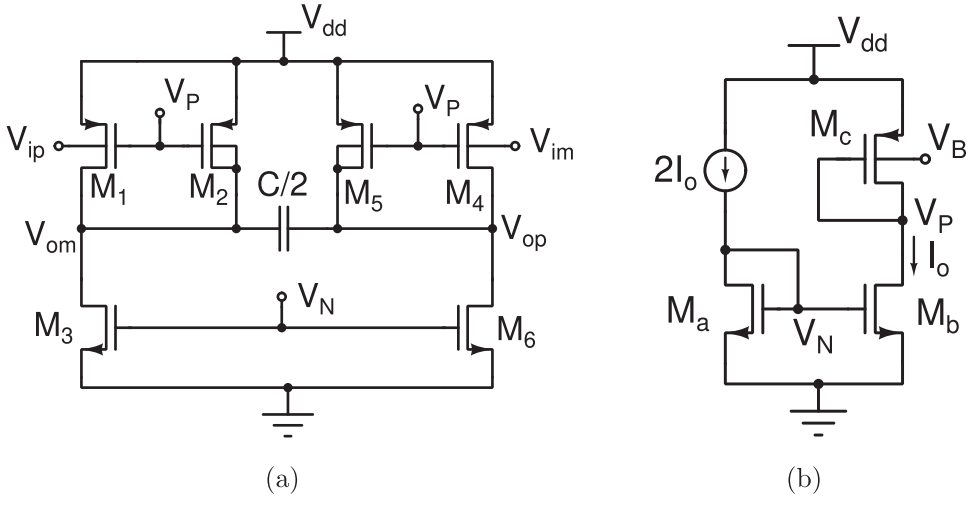


Fig. 3. (a) Fully differential configuration of the proposed BD-VF, (b) Current mirror for biasing.

Table 1
Transistor sizes in Fig. 3

Transistors	W/L (μm/μm)
M_1, M_4	24/1
M_2, M_5	21.2/1
M_3, M_6, M_a	10.6/15
M_b	5.3/15
M_c	22.6/1

$$\tau = \frac{r_x C}{1 + g_{mb2} r_x} \tag{5}$$

As $g_{mb2} r_x \gg 1$, (5) is simplified to (6) and the cutoff frequency is given by (7).

$$\tau \approx \frac{C}{g_{mb2}} \tag{6}$$

$$f_o = \frac{1}{2\pi\tau} = \frac{g_{mb2}}{2\pi C} \tag{7}$$

From Fig. 2(b), the output resistance (R_{out}) by considering $g_{mb2} r_x \gg 1$, can be written as

$$R_{out} = \frac{1}{g_{mb2}} \tag{8}$$

In (4), DC gain can be made unity, by making g_{mb1} slightly greater than g_{mb2}. Hence, sizes of M_1 and M_2 are chosen in such a way that slightly more bias current flows through M_1 than M_2.

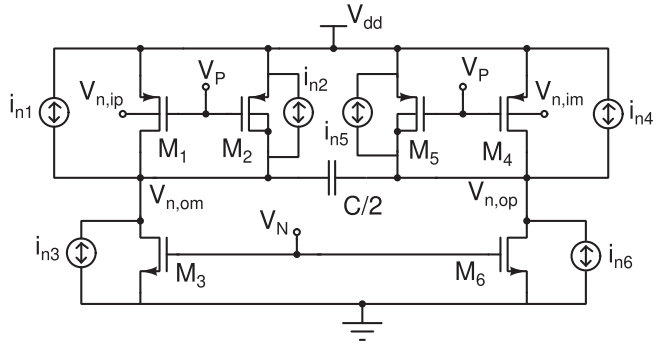


Fig. 4. Noise equivalent of proposed buffered low-pass cell.

A fully differential configuration of the proposed BD-VF is shown in Fig. 3(a). It is biased by a current mirror circuit shown in Fig. 3(b). A bias current of I_o flows through M_1, M_2, M_4 & M_5 and $2I_o$ flows through M_3 & M_6. Sizes of transistors (shown in Table 1) are chosen to ensure the sub-threshold saturation operation and for proper current mirroring. Integrating capacitance, $C/2$ is connected between the output nodes V_{op} and V_{om}.

The proposed BD-VF operates from 0.3 V supply voltage. The bulk voltages of M_c and M_1 are at input common mode of 150 mV. Since the source-gate as well as bulk voltages of M_c and M_1 are same, the current I_o is mirrored to M_1. This forces the remaining current I_o to flow through M_2. As source-gate voltages as well as drain currents of M_c and M_2 are same, and bulk and drain of M_2 are shorted together, output common mode is set to 150 mV. This circumvents the need for common mode feedback (CMFB) circuit, which is mandatory in most of the differential-in differential-out configurations.

2.1. Noise analysis

Fig. 4 shows the noise equivalent of the proposed BD-VF. It shows all transistors along with their noise sources. The power spectral density (PSD) of output voltage noise is given by.

$$\overline{v_{on}^2} = \sum_{i=1}^{6} \overline{i_{ni}^2} R_{out}^2 \tag{9}$$

where $\overline{i_{ni}^2}$ is the current noise PSD of ith transistor. The PSDs of thermal noise and flicker noise ($1/f$) of a transistor are given by (10) and (11) respectively [20].

$$\overline{i_{n,th}^2} = \frac{8}{3} kT g_m \tag{10}$$

$$\overline{i_{n,1/f}^2} = \frac{K_f}{C_{ox} WL} \cdot \frac{1}{f} \cdot g_m^2 \tag{11}$$

where k is the Boltzmann constant and K_f is the flicker noise parameter. By substituting (10) in (9), the PSD of output thermal noise voltage is given by

$$\overline{v_{on,th}^2} = \frac{8}{3} kTR_{out}^2 \sum_{i=1}^{6} g_{mi} \tag{12}$$

where g_{mi} is the transconductance of ith transistor. To make the analysis easier, the transconductance of the transistors M_1, M_2, M_4 and

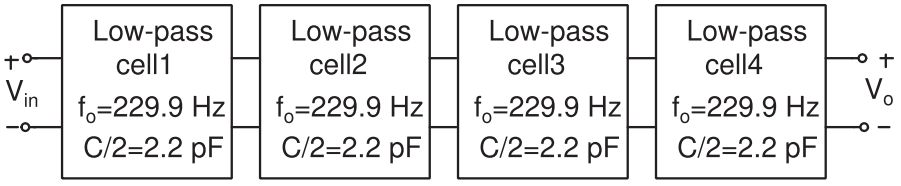
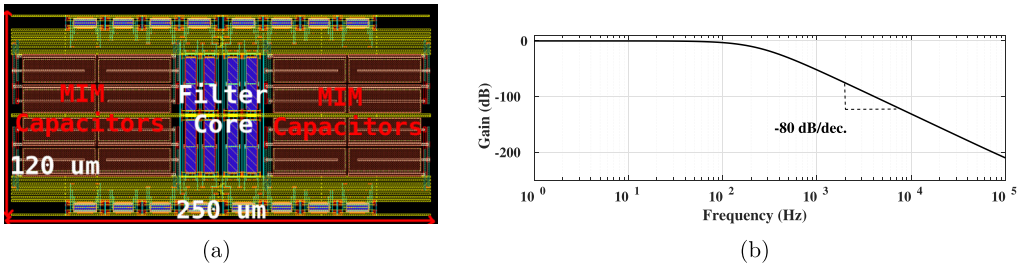


Fig. 5. 4th order LPF.



(a) (b)

Fig. 6. (a) Layout, (b) Frequency response of the filter.

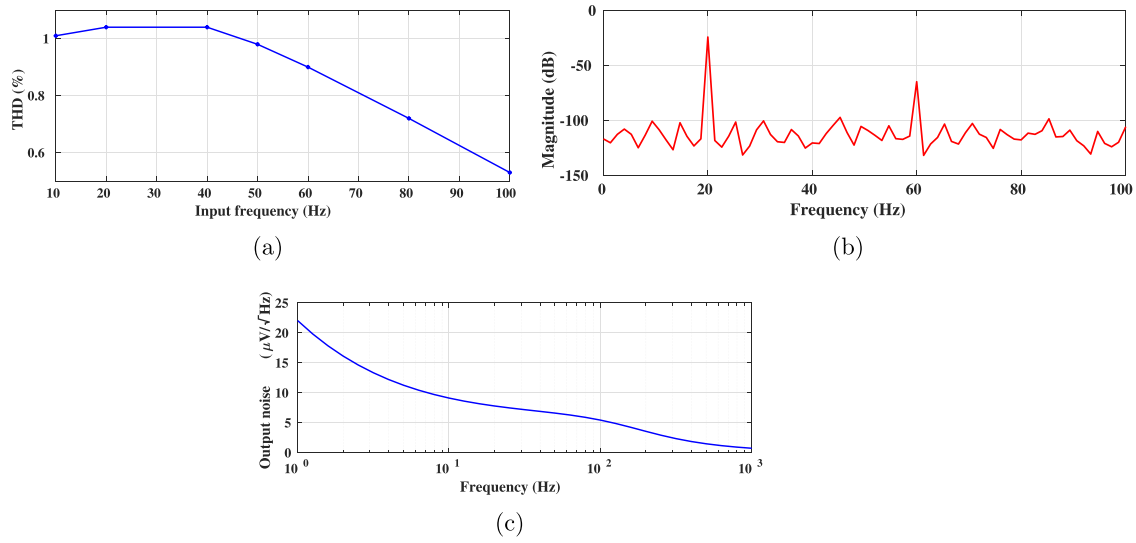


Fig. 7. (a) THD versus f_{in}, (b) Harmonics, (c) output noise of the filter.

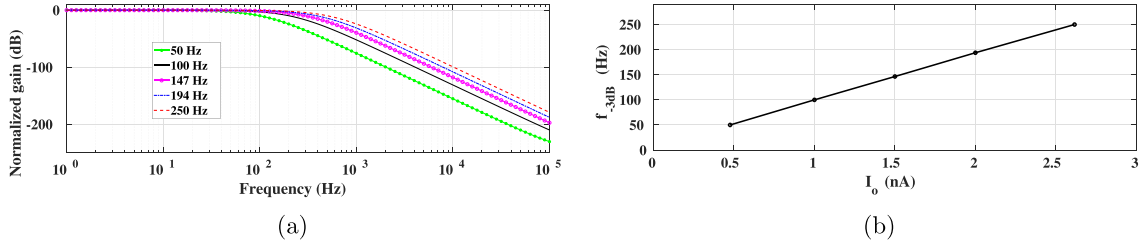


Fig. 8. (a) f_{-3dB} tuning of the filter. The results are in the format [I_o, f_{-3dB}]: [0.48 nA, 50 Hz], [1 nA, 100 Hz], [1.5 nA, 147 Hz], [2 nA, 194 Hz] and [2.6 nA, 250 Hz]. (b) f_{-3dB} versus I_o.

M_5 can be considered to be equal to g_{m2} as approximately same bias current (I_o) flows through them. Similarly, transconductance of M_3 and M_6 is considered to be equal to g_{m3}. By substituting $R_{out} = 1/g_{mb2}$ in (12),

$$\overline{v_{on,th}^2} = \frac{16kT}{3}\frac{g_{m2}}{g_{mb2}^2}\left[2+\frac{g_{m3}}{g_{m2}}\right] \tag{13}$$

By substituting (1) in (13),

$$\overline{v_{on,th}^2} = \frac{16kT}{3}\frac{1}{(\eta_p-1)g_{mb2}}\left[2+\frac{2\eta_p}{\eta_n}\right] \tag{14}$$

where η_n and η_p are the sub-threshold slope factors of NMOS and PMOS respectively. Output thermal noise power integrated over the frequency range, 0 to f_o is given by

$$P_{on,th} = \frac{32kT}{3}\frac{1}{(\eta_p-1)g_{mb2}}\left[1+\frac{\eta_p}{\eta_n}\right]\int_0^{f_o}\left|\frac{1}{1+j(\frac{f}{f_o})}\right|^2 df \tag{15}$$

$$\Rightarrow P_{on,th} = \frac{4kT}{3(\eta_p-1)C}\left[1+\frac{\eta_p}{\eta_n}\right] \tag{16}$$

Similarly, the PSD of output flicker noise voltage can be written as

$$\overline{v_{on,1/f}^2} = \frac{4}{C_{ox}(\eta_p-1)^2 f}\cdot\left[\frac{K_{fp}}{(WL)_2}+\frac{K_{fn}}{(WL)_3}\cdot\frac{2\eta_p^2}{\eta_n^2}\right] \tag{17}$$

where K_{fp} and K_{fn} are flicker noise parameters for PMOS and NMOS transistors respectively. From (17), it can be seen that the flicker noise can be reduced by increasing WL of the transistors. Hence, for the proposed design, W and L are chosen sufficiently large as given in Table 1.

Table 2
Parameters of the 4th order LPF for $I_o = 1$ nA.

Parameter	Value
Technology	UMC 180 nm
Supply Voltage (V_{dd})	0.3 V
f_{-3dB}	100 Hz
DC gain	0 dB
Tuning range of f_{-3dB}	50–250 Hz
V_{inpp} for 1% THD	130 mVpp
IRN	73 μV RMS
DR	56 dB
Power	4.8 nW
FoM	5.7×10^{-15}
Total Capacitance	8.8 pF
Active area	0.03 mm^2

2.2. 4th *order LPF*

A 4th order LPF is designed by cascading four proposed BD-VFs with same cutoff frequency. Fig. 5 shows the block diagram of the 4th order LPF whose transfer function can be written as

$$H_4(s) = \frac{1}{(1+j(\frac{f}{f_o}))^4} \tag{18}$$

where, f_o is the cutoff frequency of the first order LPF. −3 dB frequency (f_{-3dB}) of 100 Hz for the 4th order LPF translates into a cutoff frequency of 229.9 Hz for individual stages according to (19).

$$f_{-3dB} = f_o\sqrt{2^{\frac{1}{4}}-1} \tag{19}$$

Table 3
Performance comparison.

Parameter	[1][a] (2009)	[22][c] (2012)	[12][a] (2013)	[23][b] (2016)	[11][b] (2018)	[24][a] (2018)	[25][c] (2018)	[17][a] (2018)	[16][a] (2019)	This Work[c]
Technology (nm)	180	180	350	130	180	180	180	350	350	180
V_{dd} (V)	1	1	3	0.9	0.5	1	1.8	0.9	1.5	0.3
Filter order	5	2	4	2	2	5	4	4	4	4
DC gain (dB)	−10.5	0	−3.7	5.99	≈0	−7	0	−0.05	−0.09	0
Cutoff frequency (Hz)	250	76	100	48	456	250	50	100	100	100
Power (nW)	453	900	15	800	248	41	570	4.26	5.25	4.8
V_{inpp} for 1% THD (mV)	100	1220	50	7	180	100	196	70	110	130
IRN_{rms} (μV)	≈300	266	36	17.38	160	134	109	80.5	39.38	73.5
DR (dB)	50	64	66.7	43.8	52	61.2	56.1	48.2	56.9	56
Capacitance/pole (pF)	1.4	39	27.2	139	30	3.9	35.6	9.6	11.8	2.2
Active area (mm^2)	0.13	0.034	0.11	–	–	0.24	0.74	0.11	0.1	0.03
FoM ($\times 10^{-15}$)	1146	3.7 k	51.9	48.4 k	341.5	28.6	7.9 k	37.3	28	5.7

[a] Measured.
[b] Schematic simulations.
[c] Post-layout simulations.

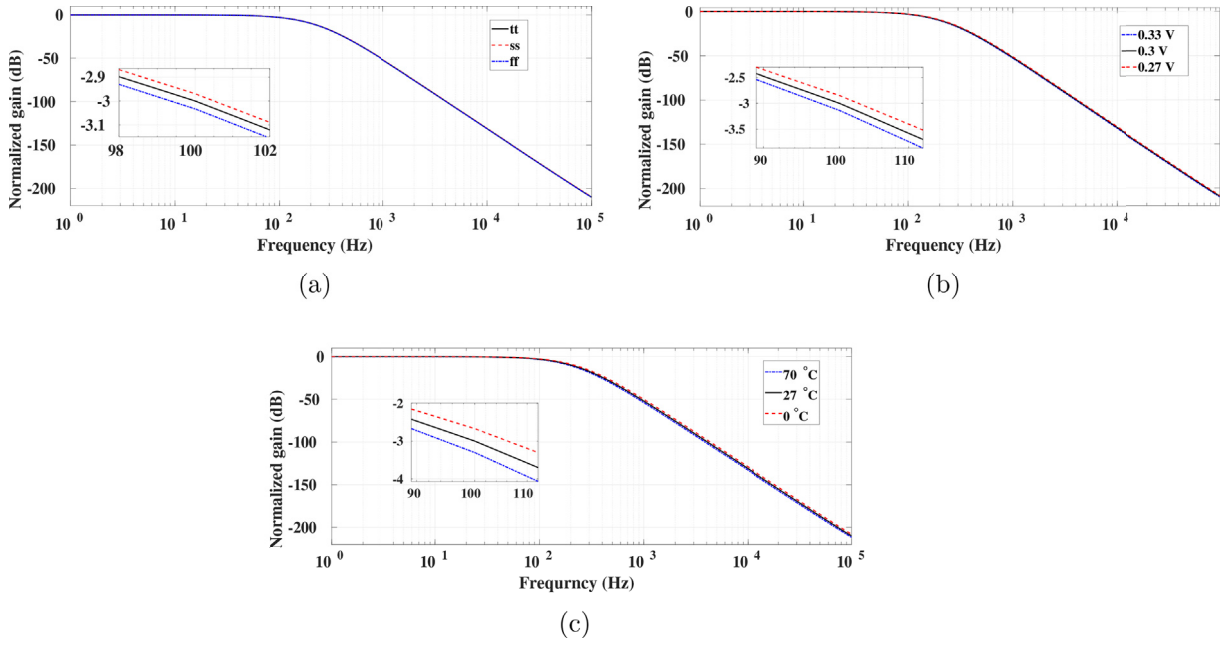


Fig. 9. Frequency response of the filter across (a) Process corners, (b) V_{dd} variations, (c) Temperature variations.

3. Post-layout results

The 4th order filter is implemented using UMC 180 nm CMOS technology and simulated in Cadence Virtuoso. The layout of the filter is shown in Fig. 6(a). It takes an area of 0.03 mm^2. Frequency response of the filter is shown in Fig. 6(b). The cutoff frequency and DC gain of the filter are 100 Hz and 0 dB respectively.

A 20 Hz sinusoidal signal is applied to the filter to check its linearity. The observed total harmonic distortion (THD) is 1% for 130 mVpp input. Further, THD is plotted against input frequency (f_{in}) as shown in Fig. 7(a). It is observed that THD is almost 1% up to an f_{in} of 50 Hz. At 100 Hz, the THD is only 0.53% as the higher order harmonics are attenuated in the stop band. Fig. 7(b) shows the output spectrum of the filter for an input signal of 130 mVpp amplitude and 20 Hz frequency. As the proposed filter is a differential structure, even harmonics are almost eliminated and only odd harmonics are present. The observed third order harmonic distortion (HD_3) is approximately −40 dB. Fig. 7(c) shows output noise of the filter. Input referred noise (IRN) integrated over the frequency range, 1–100 Hz is 73.5 μVrms. Dynamic range (DR) of the filter is found to be 56 dB. The power efficiency of the filters can be evaluated by the Figure-of-merit (FoM) defined in (20) [21].

Table 4
Summary of PVT variations.

	Process corners					V_{dd}	Temperature
	tt	ss	ff	fnsp	snfp	(±10%)	0 - 70°C
f_{-3dB} (Hz)	100	100.4	99.6	99.9	100.1	100 ± 2.8	106–95

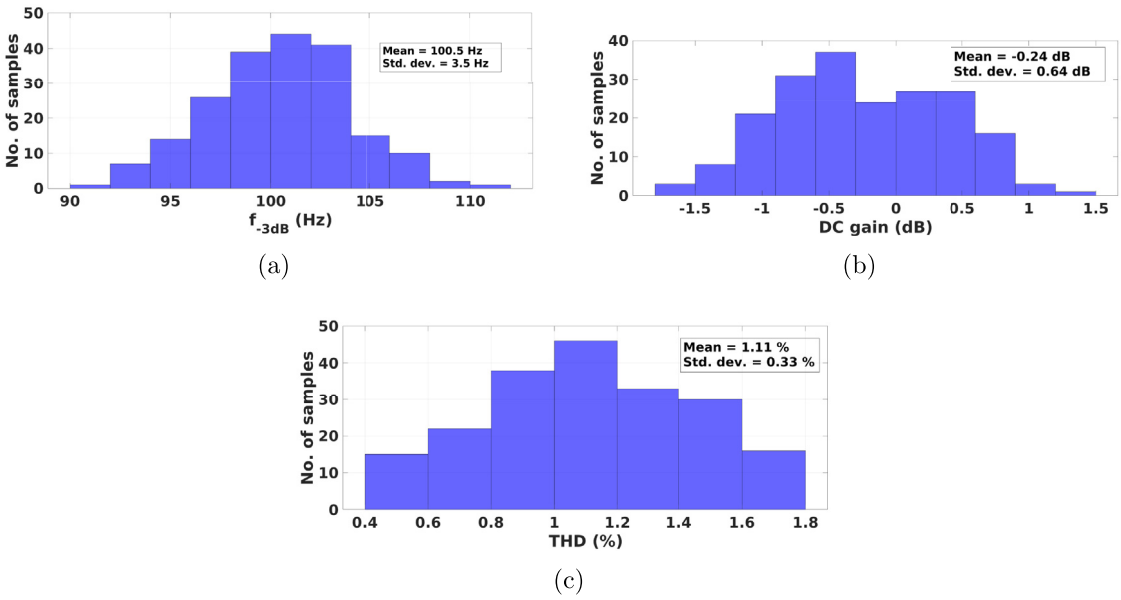


Fig. 10. Monte Carlo simulations of (a) f_{-3dB}, (b) DC gain, (c) THD.

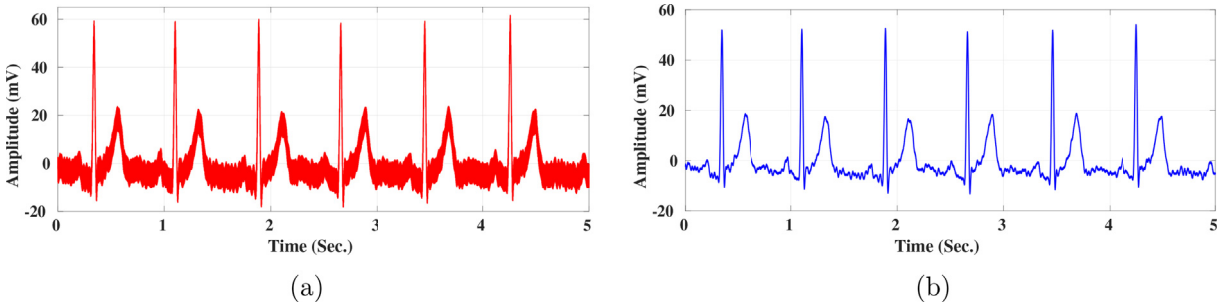


Fig. 11. ECG signal (a) before filtering, and (b) after filtering.

$$FoM = \frac{P \times V_{dd}}{N \times f_c \times DR} \tag{20}$$

where N, f_c and P are the order, cutoff frequency and power consumption respectively. Lower FoM indicates better performance. For the proposed filter, FoM is found to be 5.7×10^{-15}.

Fig. 8(a) shows the frequency response of the filter for various bias currents. The cutoff frequency can be tuned from 50 Hz to 250 Hz by varying the bias current, I_o from 0.48 nA to 2.6 nA. It increases almost linearly with I_o as shown in Fig. 8(b).

Table 2 shows the parameters of the 4th order LPF. Performance of the proposed filter is compared with other benchmark designs from literature as shown in Table 3. The proposed filter achieves a DR of 56 dB while operating with an extremely low supply voltage of 0.3 V. It shows very good performance as far as power dissipation, FoM and capacitance/pole are concerned. Power consumption is as less as 4.8 nW. FoM of the proposed filter is the least among other designs listed. Filter requires very less capacitance/pole (2.2 pF) and hence is area efficient too.

3.1. PVT and Monte Carlo simulations

The proposed filter is simulated across PVT (Process, Voltage and Temperature) variations. Fig. 9(a) shows the frequency response of the filter across process corners ('ss', 'tt' and 'ff'). f_{-3dB} is 100.4 Hz and 99.6 Hz in 'ss' and 'ff' corners respectively, which are the worst case deviations. For ±10% V_{dd} variations, the deviation in f_{-3dB} is less than ±2.8% as shown in Fig. 9(b). f_{-3dB} is 106 Hz and 95 Hz at 0°C and 70°C respectively as shown in Fig. 9(c). The summary of PVT variations is given Table 4.

Further, Monte Carlo simulations are carried out to observe the deviation in f_{-3dB}, DC gain and THD across process variations and device mismatch. Fig. 10(a), Fig. 10(b) and (c) show the histogram of f_{-3dB}, DC gain and THD respectively for 200 runs of Monte Carlo simulations. The mean of f_{-3dB} is 100.5 Hz with standard deviation of 3.5 Hz. The mean and standard deviation of DC gain are −0.24 dB and 0.64 dB respectively. The mean of THD is 1.11% with standard deviation of 0.33%.

3.2. ECG signal testing

The functionality of the proposed filter is demonstrated by filtering out-of-band noise from a noisy ECG signal as shown in Fig. 11. The noisy ECG signal (Fig. 11(a)) is generated by adding an out-of-band noise (10 mVpp, 400 Hz sinusoidal) to an ECG signal obtained from Ref. [26]. The out-of-band noise is removed by the filter as shown in Fig. 11(b).

4. Conclusion

In this paper, an extremely low voltage, low power BD-VF is presented. Fully differential configuration of BD-VF does not need any extra CMFB circuit. By using the proposed BD-VF, a 4th order LPF with cutoff frequency adjustable from 50 Hz to 250 Hz is designed for ECG signal acquisition. The filter is designed and laid out using UMC 180 nm

CMOS technology. With a capacitance/pole of 2.2 pF, the filter takes an area of 0.03 mm^2. While operating with an ultra low supply voltage of 0.3 V, the proposed filter offers a DR of 56 dB. Compared to state-of-the-art low frequency filters, the proposed filter has shown superior performance in terms of FoM, capacitance/pole and power.

Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mejo.2019.104652.

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