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A Dead-Zone-Free Zero Blind-Zone High-Speed Phase Frequency Detector for Charge-Pump PLL

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Abstract
This paper presents a novel architecture for phase frequency detector (PFD) which eliminates the blind zone effect as well as the dead zone for a charge-pump phase-locked loop (CP-PLL). This PFD is designed in 65 nm CMOS technology, and its functionality is verified across process, voltage and temperature variations. Achieved maximum frequency of operation (F_{max}) is 3.44 GHz which is suitable for high reference clocked fast settling PLLs. Proposed PFD consumes 324 μW power from 1.2 V supply at maximum operating frequency. The area occupied by proposed circuit layout is 322.612 μm^2.

Keywords Phase frequency detector · Blind zone · Dead zone · Low power · Phase-locked Loop · High speed

1 Introduction

With advancements in CMOS technology, more and more sophisticated electronic systems are being implemented. Most of these systems demand low-power high-speed phase-locked loops (PLL) for clock synchronization, clock and data recovery (CDR), frequency synthesis, etc [1]. Charge-pump PLL (CP-PLL) is a commonly used PLL architecture which allows to use passive loop filter and can easily track phase and frequency errors [3,9]. Block diagram of a CP-PLL is shown in Fig. 1.

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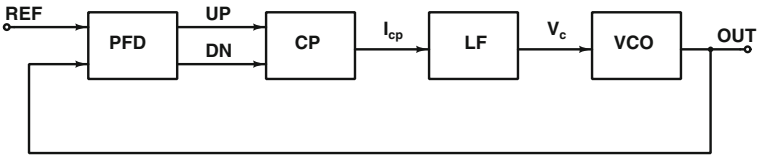

Fig. 1 Block diagram of CP-PLL

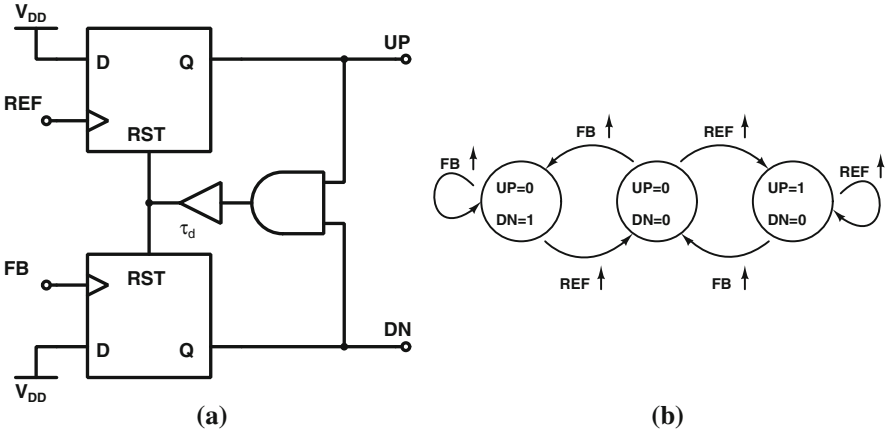

Fig. 2 Conventional phase frequency detector **a** schematic, **b** state diagram

CP-PLL is a negative feedback system which consists of phase frequency detector (PFD), charge pump (CP), loop filter (LF) and voltage-controlled oscillator (VCO). Phase error detection is an important task performed by PFD in the CP-PLL. PFD compares the phase and frequency of the reference input and the feedback taken from VCO output and generates UP and DN signals. These UP and DN signals drive the CP which sources or sinks the current I_{cp} into/from LF. The LF filters out high-frequency components and generates a control voltage V_c for VCO which is proportional to the phase error between the reference and feedback signal. V_c drives the VCO output frequency in the direction of reducing the phase error. When reference and feedback signals match, LF generates constant V_c and the loop is said to be locked. By connecting a frequency divider (divide by "N" network) in the feedback path, which takes the input from VCO output and gives its output to PFD, PLL output frequency can be made "N" times the reference signal frequency when it is in locked state.

As the reference frequency of the PLL increases, conventional PFD designs show degrading performance due to dead zone and blind zone issues. Block diagram of a conventional PFD is shown in Fig. 2 with its state diagram [11].

Initially, say REF rises and UP goes high then as soon as FB rises DN signal goes high and reset path is activated, so both UP and DN are pulled down. This operation generates a reset pulse whose width is decided by RST-to-Q delay of D-flipflop, AND gate delay and an extra delay (τ_d) due to the delay element added to achieve dead-zone-free operation. When the loop is locked, if reset pulse width is not enough to turn on CP, then PLL will be in open loop for small phases which increases the phase noise

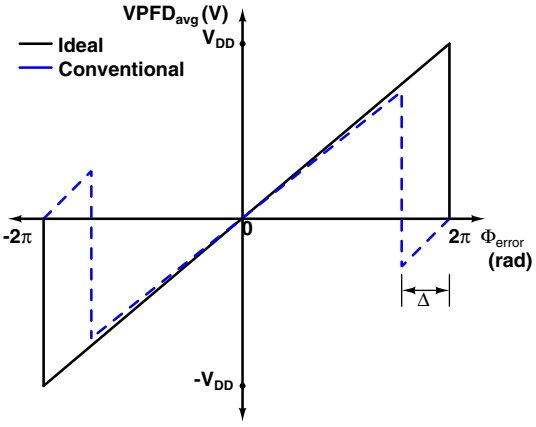

Fig. 3 Comparison of PFD characteristic

or jitter [13]. Minimum width of the reset pulse (T_{rst}) is decided by the settling time of the CP. A high-speed PFD design demands smaller reset pulse. However, wider reset pulse helps in removing the dead zone which helps in avoiding open-loop condition in PLL. But this increases the blind zone and limits the maximum operating frequency. Maximum operating frequency is related to T_{rst} as given in (1) [14].

$$F_{\max} = \frac{1}{2\,T_{\text{rst}}} \tag{1}$$

Ideally, PFD phase error detection range is from -2π to $+2\pi$. However, due to the blind zone effect, it reduces from $-2\pi + \Delta$ to $2\pi - \Delta$ as shown in Fig. 3 where Δ is given by the following expression (2).

$$\Delta = 2\pi \cdot \frac{T_{\text{rst}}}{T_{\text{REF}}} \tag{2}$$

In blind zone area, PFD misses the correct rising edge and detects the upcoming rising edge which is lagging. Due to this wrong phase error, cycle slipping happens during PLL lock acquiring operation. This will increase the lock time of the PLL. Hence, it is challenging to design efficient PFD circuit block for high-speed PLLs. In the literature, many circuit techniques are presented which can remove dead zone as well as blind zone, but they have limitation on maximum operating frequency [6,15]. Some designs use delay elements to introduce a delay equal to T_{rst} at the input to push the rising edge outside the blind zone. However, blind zone is still present in these designs due to PVT variations [2]. There are nonlinear PFD architectures which remove the blind zone by saturating the PFD characteristic in -2π to $-\pi$ and $+\pi$ to $+2\pi$ range. In these designs, although capture range is reduced to 2π, $F_{\max}$ achieved is found to be less than 2.15 GHz [5,7]. There are some techniques achieving high frequency of operation without using any reset mechanism. However, minimal dead zone and blind zone are still found to be present [12].

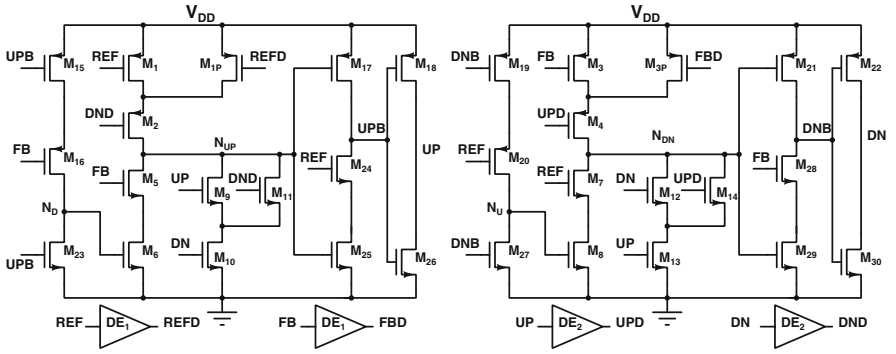

Fig. 4 Proposed phase frequency detector

In this paper, a low-power dead-zone-free, zero blind-zone high-speed PFD is presented. PLL with the proposed PFD can operate up to 3.44 GHz with a power consumption of 324 μW. The paper is organized as follows. Section 2 describes the detailed architecture and post-layout simulation results of the proposed PFD. Comparison of the results with state-of-the-art designs is also given. Implementation of the CP-PLL with the proposed PFD is explained in Sect. 3. Conclusion is drawn in Sect. 4.

2 Proposed Phase Frequency Detector

Figure 4 shows the circuit diagram of the proposed phase frequency detector. It is a modified version of the circuit presented in [6]. It is a kind of true single-phase clock (TSPC) logic which is modified for the intended functionality. In a conventional PFD, reset signal operates for all phase and frequency comparison. Proposed PFD generates reset pulses only during dead zone, when the normal operation of the PFD is not able to detect the phase error. Basically, during normal operation mode, this PFD generates UP or DN signal proportional to a leading or lagging phase error between reference (REF) and feedback (FB) signals, respectively. During the dead zone region, both UP and DN signals are generated and phase error is an average of it, as usually done in the conventional PFD.

During normal operation, nodes N_{UP} and N_{DN} charge to V_{DD} through main pull-up networks consisting of transistors M_1, M_2 and M_3, M_4, respectively. Main pull-down paths for these nodes are through transistors M_5, M_6 and M_7, M_8, respectively. Additional pull-down paths are added to these nodes through transistors M_9–M_{11} and M_{12}–M_{14} as shown to generate the reset pulse which helps to remove the dead zone from the circuit. Pre-charge transistors M_{1P} and M_{3P} are added in parallel with M_1 and M_3 to remove the blind zone that otherwise occurs due to the pre-charge time required by the decisive nodes N_{UP} and N_{DN}. Delay elements (DEs) are used to get delayed versions (REFD, FBD, UPD and DND) of signals REF, FB, UP and DN. UPD and DND signals are used for the stability of the PFD circuit, while REFD and FBD signals are used for removing blind zone effect. Proposed circuit is designed

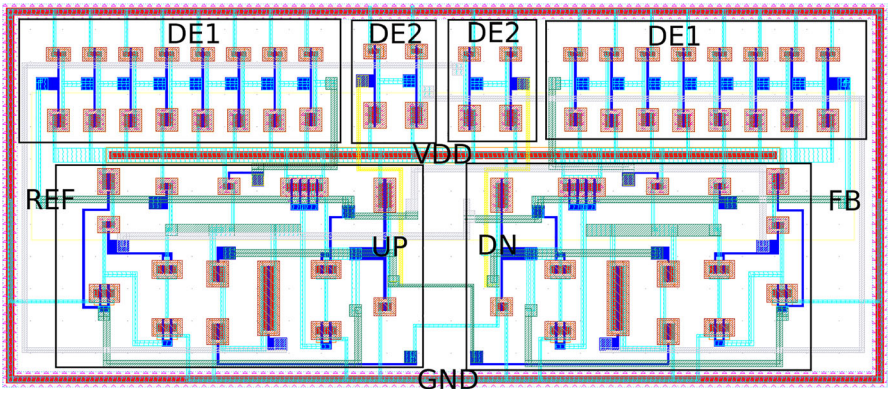

Fig. 5 Layout of proposed PFD

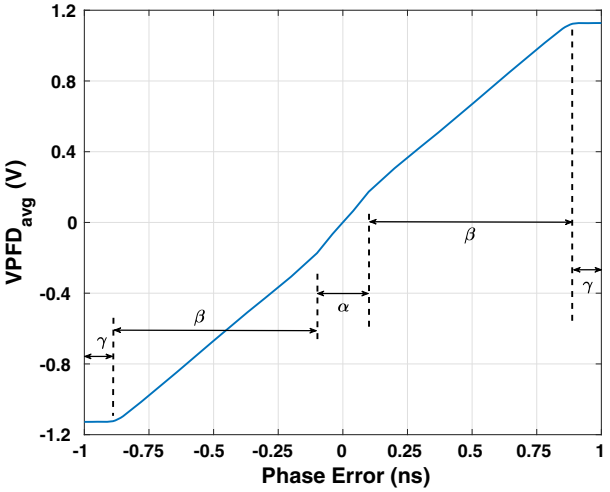

Fig. 6 Characteristic of proposed phase frequency detector @ 1 GHz

and implemented in 65 nm CMOS technology. Layout of the circuit shown in Fig. 5 occupies an area of $322.6\,\mu m^2$.

Post-layout characteristic of the proposed PFD is shown in Fig. 6 where region α is the dead zone area where the PFD generates both UP and DN pulses just like the conventional PFD. In region β, phase error information is contained in only one signal UP or DN as they are not high together, i.e., when UP is high, DN is low and vice versa. Region γ is a saturated area which avoids a phase inversion using a pre-charge path through M_{1P} and M_{3P} transistors. Operation of the proposed PFD is explained as follows.

Initially, during reset state (UP = DN = 0) when REF, FB and delayed signals UPD and DND are low, nodes N_{UP} and N_{DN} go high through main pull-up paths. If the signal REF makes a transition from low to high, node UPB is pulled down through transistors M_{24}–M_{25} and UP goes high. This causes node N_{DN} to discharge through

transistors M_{13} and M_{14}, and hence, node DNB charges to V_{DD} and DN goes low. With this, node N_D charges to V_{DD} through transistors M_{15} and M_{16} and PFD is in state UP = 1 and DN =0. Main pull-up path for charging node N_{DN} is disabled due to high signal on UPD at the input of transistor M_4. During this state, any transition on REF will not change the state of PFD. If the signal FB makes a transition from low to high, node N_{UP} discharges through M_5 and M_6 and UPB gets pulled high and UP goes low. As node N_{DN} was discharged when UP = 1, there is no transition on DN signal. In this way, PFD changes its state from UP = 1, DN = 0 to UP = 0, DN = 0 without any extra reset circuit which will happen only when phase error between REF and FB is greater than the dead zone area and falls in region β. A similar analysis can be done for the state changing from UP = 0, DN = 1 to the reset state UP = 0, DN = 0 when FB signal makes a transition to high before REF.

If the phase error between REF and FB signals falls in the dead zone, nodes N_{UP} and N_{DN} both get pulled high making UP and DN also high. Rising edges of both UP and DN signals contain input phase error information. As soon as both the signals go high, nodes N_{UP} and N_{DN} are pulled down by transistors M_9, M_{10} and M_{12}, M_{13}, respectively. Width of the reset pulse is decided by these pull-down transistors. In [6], phase error detected in the dead zone area is twice the input phase error. This is due to the rising edge of UP or DN signal, whichever goes high first will pull down the other signal by the same amount of time faster. Hence, falling edge of slower signal happens earlier. Due to this, falling edge of both the signals gets the same phase error again. Hence, average of UP and DN signals will be two times the input phase error which degrades the performance of PLL in locked condition. This limitation is eliminated in the present work. If input phase difference falls in the region γ, pre-charge network is used with delayed signals REFD and FBD which will avoid the phase inversion in the characteristic.

Post-layout simulation is done across all process corners for normalized characteristic of the proposed PFD, and the same is shown in Fig. 7. Across all the corners, characteristic is found to be consistent.

Transient simulations are done for various cases of phase error occurrence which verify the functionality of the proposed PFD. Figure 8 shows the phase error detection at an operating frequency of 1 GHz where a phase error less than half a period is applied to PFD. It is seen from Fig. 8a that when REF leads, UP signal goes high and DN goes low, while Fig. 8b shows the case when FB leads, DN goes high and UP goes low. Hence, both UP and DN signals carry the phase error information in terms of pulse width of a signal which can be seen in respective figures.

Similarly, phase error greater than half a period applied at 1 GHz operating frequency is verified from Fig. 9 for both the leading and lagging phase error between PFD inputs. Figure 10 represents the dead zone operation at 1 GHz operating frequency. When the phase difference between REF and FB signals falls in the dead zone (region α), both UP and DN signals are generated like the conventional PFD. Two cases with zero and 10 ps phase errors are considered, and the corresponding UP and DN signals are plotted in Fig. 10a, b, respectively. It can be seen that the proposed PFD can detect the smallest phase error efficiently.

Blind zone operation is shown in Fig. 11a, where the phase error falls in region γ. It can be seen that UP signal falls when FB rises, but then, when REF rises again,

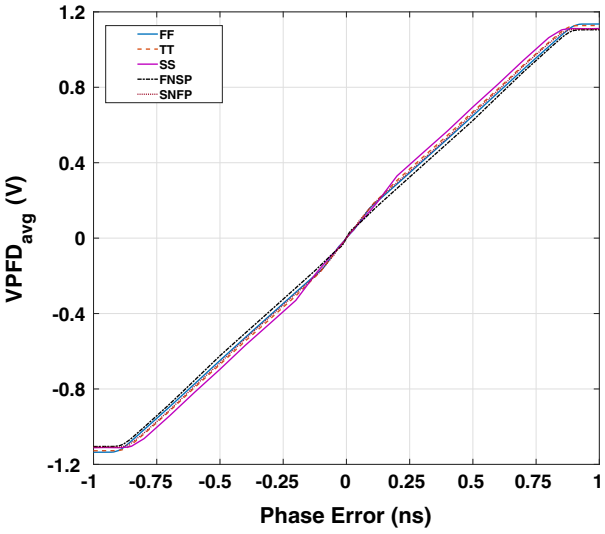

Fig. 7 Proposed PFD characteristic simulated across all corners @ 1 GHz

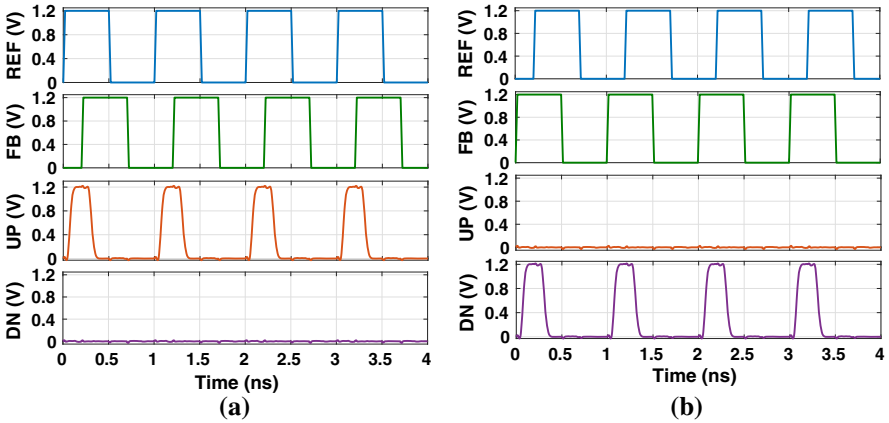

Fig. 8 Phase error between REF and FB less than $T/2$ @ 1 GHz **a** leading REF, **b** leading FB

UP does not reach the ground completely, instead, it rises. In conventional PFDs, this second rising edge of REF signal will be missed and upcoming rising edge of FB signal will be considered which is a wrong phase information that can increase the cycle slipping in PLL while acquiring lock. Hence, the pre-charge network consisting of transistors M_{1P} and M_{3P} eliminate the blind zone and as shown in Fig. 11a. Figure 11b verifies the phase error detection for a variable input frequency applied to the proposed PFD.

Figure 12a shows the maximum frequency of operation ($F_{\max}$) as the supply voltage is varied. It can be seen that the PFD can operate at supply voltage as low as 0.6 V. However, the $F_{\max}$ offered reduces to 0.5 GHz. In many SoCs, it is preferred to operate PFD on low supply voltages for saving on the power. For such requirements, the

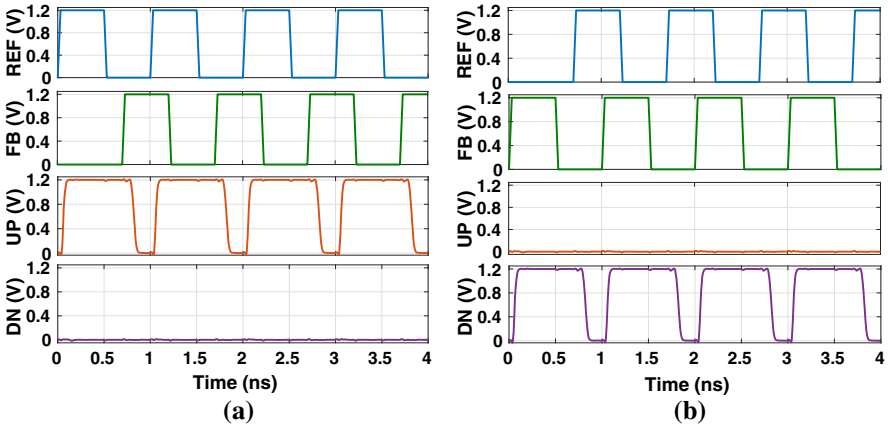

Fig. 9 Phase error between REF and FB grater than $T/2$ @ 1 GHz, **a** leading REF, **b** leading FB

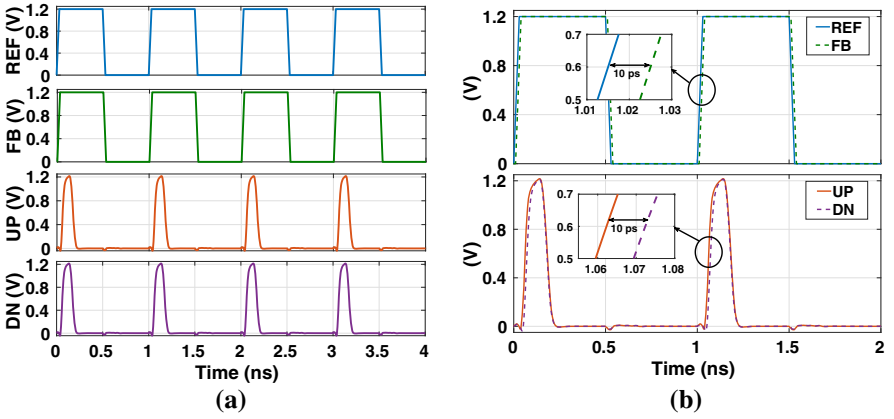

Fig. 10 Phase error between REF and FB @ 1 GHz, **a** zero phase error, **b** REF leads by 10 ps

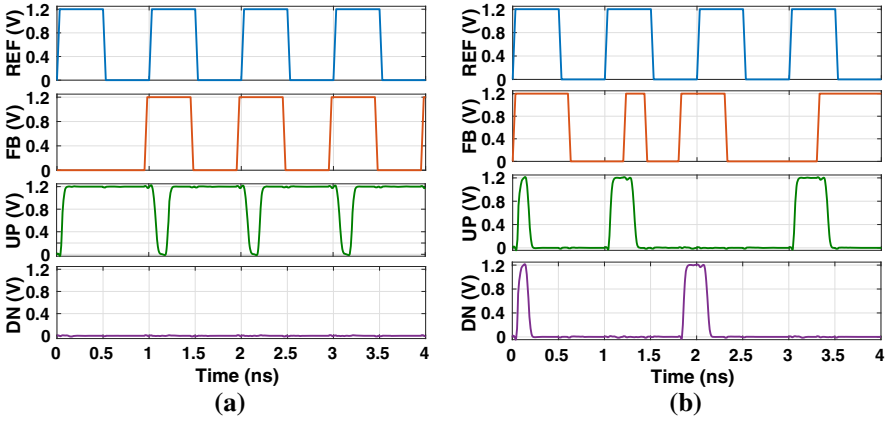

Fig. 11 **a** REF leads FB by 950 ps phase @ 1 GHz, **b** Phase error detection for different frequencies

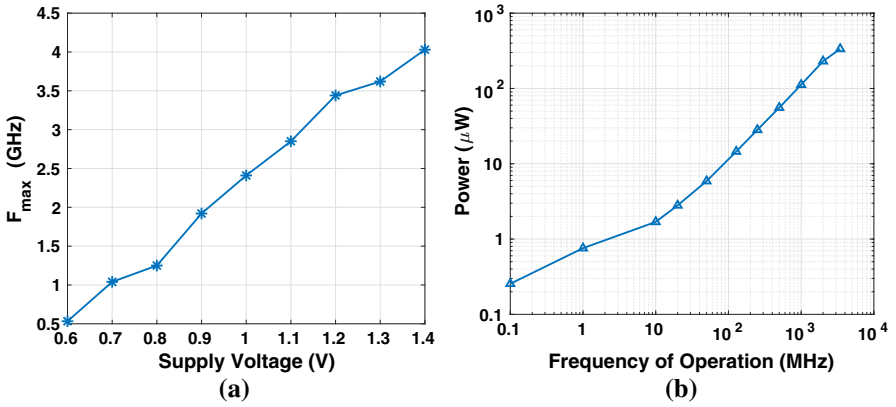

Fig. 12 **a** Maximum frequency of operation versus supply voltage, **b** power consumption for various frequencies of operation

Table 1 Post-layout simulation across process corners and temperature for nominal supply voltage (1.2 V)

Corners	Temperature (°C)	Reset time (ps)	$F_{\max}$(GHz)	Power @ $F_{\max}$ (μW)
TT	− 40	135	3.7	353
	27	145	3.44	324
	125	170	2.94	314
FF	− 40	115	4.35	473
	27	138	3.62	437
	125	160	3.12	360
SS	− 40	185	2.7	265
	27	215	2.32	251
	125	246	2.03	236
FNSP	− 40	148	3.37	357
	27	160	3.12	340
	125	184	2.72	305
SNFP	− 40	161	3.1	344
	27	181	2.76	311
	125	201	2.48	283

proposed PFD could be a potential candidate. Figure 12b plots the power consumption for various operating frequencies. It shows that the proposed PFD consumes power in nW to μW range at nominal voltage of 1.2 V. Table 1 shows various parameters of the proposed PFD across process corners and temperature variations. Results indicate promising performance of the proposed PFD.

Comparison of proposed PFD (typical PVT case) with previously published PFD designs is listed in Table 2. Though design in [12] has higher operating frequency, it suffers from both dead zone and blind zone. Although designs given in [6,7,15] are free from dead zone and blind zone, their power consumption is on the higher side and

Table 2 Comparison of proposed PFD with recently published work

Parameter	Technology (nm)	V_{DD} (V)	Dead zone	Blind zone	F_{max} (GHz)	Power (μW)
[6]*	180	1.8	Free	Free	1.5	1360 @1 GHz
[4]*	130	1.2	80 ps	120 ps	3	134 @128 MHz
[7]†	180	1.8	Free	Free	2.15	0.27 @20 MHz
[2]‡	130	1.2	Free	61 ps	2.94	496 @128 MHz
[10]*	180	1.8	Free	150 ps	3.33	110 @3.33 GHz
[12]†	130	1.2	25 ps	minimal	4.1	76 @4.1 GHz
[15]*	130	1.2	Free	Free	2	1440 @1 GHz
[5]†	65	1.2	–	Free	1	134 @1 GHz
Conventional†	65	1.2	Free	500 ps	1	185 @1 GHz
Proposed†	65	1.2	Free	Free	3.44	324 @3.44 GHz

‡Fabricated; †post-layout simulation; *schematic simulation

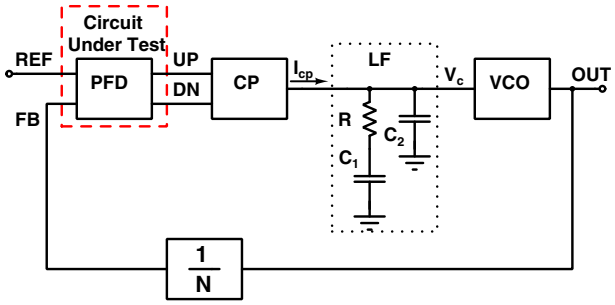

Fig. 13 Test-bench schematic of CP-PLL

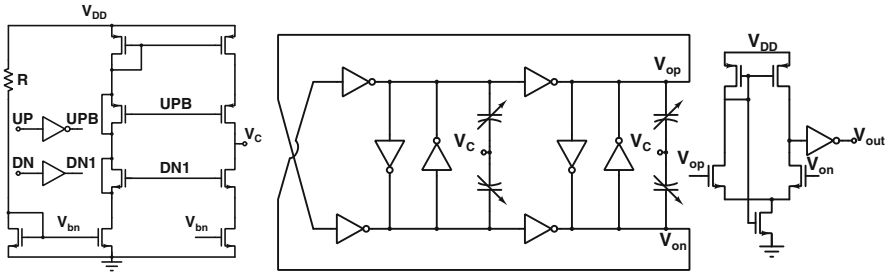

Fig. 14 Schematic diagram of **a** Charge pump, **b** voltage-controlled oscillator

F_{max} achieved are less than the proposed work. Design in [5] is blind-zone-free and consumes comparable power. However, F_{max} achieved in this design is only 1 GHz.

3 Charge-Pump PLL with Proposed PFD

To ascertain the use of proposed PFD in PLL and to prove its effect on the PLL performance a type II, third-order CP-PLL is implemented using the proposed PFD and the performance is evaluated at high operating frequency. The test-bench schematic of the CP-PLL is shown in Fig. 13 where passive second-order loop filter (LF) is implemented with one resistor and two capacitors as shown.

Schematics of the basic CP and pseudo-differential ring oscillator-based VCO used in the simulation of PLL are shown in Fig. 14. Charge pump is designed for a sourcing/sinking current of 100 μA. VCO is designed to have a gain of 1 GHz/V. To compare the proposed PFD with conventional PFD using the same test-bench, conventional NAND latch-based D-flipflop [8] is implemented in 65 nm CMOS technology. Similar D-flipflop is used for implementing frequency divider circuit too in the feedback path to divide the VCO frequency by two.

Transient simulation is carried out by verifying the PLL lock acquisition process. Lock acquisition with proposed and conventional PFDs for output frequency of 1 GHz are shown in Fig. 15. Note that, the frequency chosen at 1 GHz due to the limitation

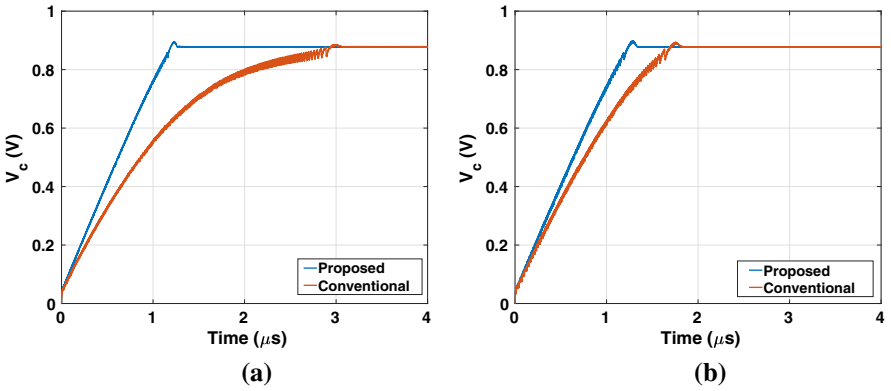

Fig. 15 Lock acquisition of 1 GHz PLL for **a** $F_{\text{ref}} = F_{\text{out}}$ **b** $F_{\text{ref}} = F_{\text{out}}/2$

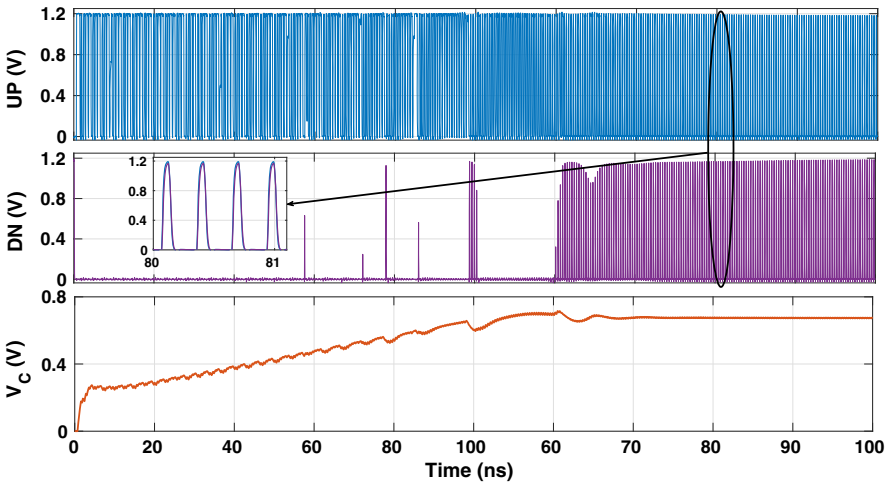

Fig. 16 Operation of PLL at 3.44 GHz (F_{max}) reference frequency ($N = 1$)

posed by conventional PFD. In the first case, a reference frequency of 1 GHz is applied without dividing the frequency ($N = 1$) in the feedback path. It can be seen that the PLL with proposed PFD shows excellent performance with a settling time of 1.28 µs when compared to the conventional PFD which settles at 3.08 µs. Hence, with the proposed PFD, loop gets locked 1.8 µs faster than with conventional PFD (Fig. 15a). In the second case (Fig. 15b), reference frequency of 500 MHz is applied with a frequency division of 2 ($N = 2$) in the feedback path. In this case also, PLL with proposed PFD performs better than with conventional PFD, i.e., locking happens around 500 ns faster. It is observed from Figure 15 that at higher frequencies conventional PFD is having more cycle slipping due to the blind zone effect while the PLL with the proposed PFD is taking approximately the same locking time.

To verify the performance of the proposed PFD when PLL is running at reference frequency of 3.44 GHz (F_{max}), same test-bench setup is used with VCO designed for a

tuning range which includes F_{max}. Loop filter parameters are also updated accordingly. Transient simulation of PLL acquiring lock condition at F_{max} frequency is shown in Fig. 16. It can be seen that PLL is locking within 70 ns and UP-DN pulses are generated to overcome dead zone issue in locked condition so that PLL gets locked and track the reference frequency simultaneously. Zoomed portion in Fig. 16 shows that the UP and DN pulses are overlapped with minimal steady state phase which is caused by charge-pump mismatch current in locked state.

4 Conclusion

In this paper, a novel dead-zone-free, zero blind-zone high-speed PFD is presented. This PFD is proved to avoid cycle slipping, while PLL locking process and can work up to 3.44 GHz operating frequency making it suitable for high reference PLL, DLL and CDR applications. The proposed PFD offering 3.44 GHz F_{max} with power 324 μW operating on nominal supply is found to be a promising architecture. With some fine tuning, F_{max} can further be increased.

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