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A Fixed Frequency Duty-Ratio Based Digital Sliding-Mode Controller for DC–DC Buck Converter

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The hysteresis modulation (HM) based sliding mode control (SMC) implementation results in variable frequency, where the converter's operating frequency cannot be measured accurately. This will have a negative impact on circuit component and filter design. Furthermore, it is sensitive to the disturbances and the parameter uncertainties. To maintain constant switching frequency during line and load regulation, a duty-ratio (DR) based sliding-mode (SM) control approach is proposed in this paper and applied to a DC–DC buck converter. The translation of the SM control law for HM and DR scheme implementation by using field programmable gate array (FPGA) for DC–DC buck converter is illustrated. A simple and self-explanatory design and implementation procedure are also addressed. The performance and robustness of the proposed DR-based SM controllers are validated by both simulation results using MATLAB/Simulink and experimental results. The robustness of the SM controller is tested at various operating conditions and compared the results with HM-based SM and conventional linear controller.

Keywords: DC–DC Converter, Digital Controller, Hysteretic Control, Nonlinear Controller, Sliding-Mode (SM) Control.

1. INTRODUCTION

Switched-mode voltage regulators are required for the applications such as battery charging, complex communication systems, automotive control circuits and micro-controller circuits. These applications demand good voltage regulation at the output and, having fast dynamic response under sudden load fluctuation and input supply variation. The controller demands to sense the feedback states to compensate the system disturbance and to generate gate pulses for the DC–DC converter.[1] The control of converter using conventional linear controllers such as proportional-integral (PI) and proportional-integral-derivative (PID) are designed based on the small-signal analysis. It is essential to determine converter transfer function to find gain coefficients of the linear controllers using special techniques such as pole-placement, Eigen value and frequency domain methods.[2,3] These controllers failed to perform satisfactorily during the circuit component variations or parametric uncertainties (known as a large-signal variation) as it is optimized for a specific condition.[4] Moreover, it suffers from high peak overshoot and more settling time under parametric variations.[5,6] This demands a non-linear controller with variable structure systems (VSS) which can provide robustness and good dynamic response for the wide variation of circuit parameters.

Sliding-mode (SM) controllers are one type of non-linear controller and known for controlling VSSs.[7] Recently, a lot of research towards the application of SM controllers to power converters due to their guaranteed stability and the robustness against parameter, line, and load variations.[8,9] Moreover, it has a high degree of flexibility in its design choices, large signal stability, resilient to parametric variations and relatively easy implementing as compared with other types of non-linear controllers.[10,11] Earlier in theoretical works, the focus is on SM control method for second-order[12] and fourth-order DC–DC converters.[13] To increase the robustness, an adaptive back-stepping[14] and the integration of SM controller with passivity-based controller[15] is carried out. Similarly, integration with the neural networks to increase the power factor of the DC–DC converter is presented in Ref. [16]. The theoretical and robustness comparison

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between proportional-integral (PI), fuzzy-logic and SM controller for DC–DC buck converter is addressed in Refs. [10, 17] and observed the similarity between SM and fuzzy-logic controller. Most of the research is focused on DC–DC converter design and performance rather than the hardware implementation procedure.

The conventional approach of implementing the SM controller uses hysteresis modulation (HM) which is basically a type of signum function and realized by a switch relay.[18] Analysis, design issues with associated practical challenges of the SM controller[19] and start-up control[20] for DC–DC buck converter in continuous conduction mode (CCM) operation is reported. A time-optimal SM controller based on Pontryagin's minimum principle for buck converter is proposed to improve the dynamic response.[21] A low-cost implementation of the SM control using analog circuitry,[20] hybrid analogue-digital controller[22] and integrated circuit (IC) based on complementary metal-oxide semiconductor 130 nm technology are reported in Ref. [23]. The implementation of SM control law using above methods[19–23] results in uncontrolled and high frequency under the parametric variations. This may leads to increase in converter losses, electro-magnetic interferences (EMI) and oversized design of the input and output filters.[24] Hence, it is desirable to operate at a constant switching frequency for SM controlled DC–DC converters.

To keep at a fixed switching frequency in HM-based SM controllers during supply fluctuations and load variations, incorporation of constant timer circuits,[25] variable width hysteresis comparator,[26] adaptive feed-forward control based hysteresis band[27] and injection of a fixed-frequency external signal to the switching surface.[28] However, these approaches need additional circuitry, deterioration of transient response under load variation and its implementation is nontrivial. Other approaches to maintain the switching frequency of SM controllers by changing modulation methods such as pseudo sliding-mode (PSM)[29] and pulse width modulation (PWM).[30, 31] The implementation of these controllers using analog circuitry and micro-controllers is addressed in the literature.[32, 33] These approaches are sensitive to analog component drifts, difficulty in implementation sophisticated control laws and require error-budgeting for proper operation.[34] The digital implementation overcomes component sensitivities and deserves a high degree of re-programmability. The digital control for DC–DC converters by using FPGA are introduced in Refs. [35, 36]. The implementation of different linear controllers using a FPGA are compared and concluded that the digital controller is better than the analog controller in respect of robustness and stability.[37]

Recently, researchers are focused on digital control performance improvements for DC–DC converters due to advances in the digital controller technologies. A labview-based implementation with a reduced order observer model for buck converter is presented based on PWM strategy.[38] However, due to the complexity in the control algorithm, its switching frequency is limited to 3.6 kHz. In Ref. [39], a linear discrete-time model is derived with three digital controllers for output voltage regulation. Even though the designed controller presents an excellent performance under load and line variations, this approach requires complex tuning of gain coefficients. A variable hysteresis control strategy is proposed in Ref. [40] which require additional controllers to operate at constant switching frequency and for stability. A linearized discrete-time model derived from small-signal model of the converter utilizing sliding mode theory for synchronous buck converter is presented in Ref. [41]. It is to be noted that a discrete-time model used for digital implementation, therefore it is consistent with the type of implementation. However, this approach uses PI controller for outer loop voltage control for synchronous buck converter, which require tuning of the gain coefficients and bandwidth issues.

This paper presents a duty-ratio controlled sliding mode (DR-SM) digital controller with constant switching frequency for a DC–DC buck converter. The proposed method utilizes on-line calculation of gain coefficients and does not require any tuning of PI controllers as well as additional circuitry for maintaining constant switching frequency and the stability. The proposed method is validated by simulations in MATLAB/Simulink and shows the capability of stabilized output over the wide operating range of disturbances. The hardware design and implementation methodology along with performance comparison of SM controller in the digital platform are missing in the literature. A step-by-step and self-explanatory implementation procedure for digital control using FPGA is also depicted. Experimental results on a practical DC–DC buck converter with digital control using FPGA is presented to further validate the proposed scheme.

2. GENERAL DESIGN OF SLIDING-MODE VOLTAGE CONTROLLER FOR DC–DC BUCK CONVERTER

SM controller design for buck converter requires the state space averaging model of the system. The state space averaging model is derived on the condition of buck converter working in CCM. The state variables output voltage error x_1 and capacitor current x_2 (rate of change of x_1) can be represented as shown in Figure 1:[15]

$$x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} x_1 \\ \dot{x}_1 \end{bmatrix} = \begin{bmatrix} V_{\text{ref}} - \beta V_0 \\ \dfrac{\beta}{C}\left[\dfrac{V_0}{R_L} - \displaystyle\int\left(\dfrac{uV_{\text{in}} - V_0}{L}\right)dt\right] \end{bmatrix} \quad (1)$$

Where V_{in}, V_{ref}, βV_0 are the input, reference and sensed output voltage, respectively. R_L, L and C are the load resistance, inductance and capacitance respectively; i_L, i_C and i_R are inductor, capacitor and load currents of the buck converter. The switching value of converter is denoted

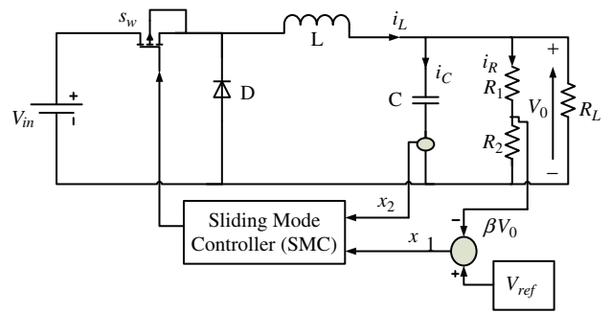


Fig. 1. Block diagram of the sliding mode controller for DC–DC buck converter.

as u_{sw}. The switching value ($u = 0$ or 1) is obtained by the following function:[11]

$$u = u_{sw} = \frac{1}{2}(1 + \text{sign}(\sigma(x))) = \begin{cases} u^+ = 1, & \sigma(x) > 0 \\ u^- = 0, & \sigma(x) < 0 \end{cases} \quad (2)$$

The phase trajectories of buck converter for two different structures of buck converter, the phase trajectories will approach towards the balanced point ($V_{ref} - \beta V_0$) during the ON(u^+) as shown in Figure 2(a). The phase trajectories will reach towards the balanced point (V_{ref}) during the switch is OFF(u^-) as shown in Figure 2(b). The state space equations of a buck converter is given by

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -\frac{1}{LC} & -\frac{1}{R_L C} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{\beta V_{in}}{LC} \end{bmatrix} u + \begin{bmatrix} 0 \\ \frac{V_{ref}}{LC} \end{bmatrix} \quad (3)$$

The fundamental concept of SM control law is to design a sliding surface, for which the phase trajectories of state variables are directed towards the equilibrium point. The instantaneous values of phase trajectory $\sigma(x)$ are given by:[7]

$$\sigma(x) = k_1 x_1 + k_2 x_2 = 0 \quad (4)$$

The designer should select the sliding co-efficients k_1 and k_2, so that the controller satisfies hitting, existing and stability condition for all operating input voltages and load currents of the DC–DC buck converter. With the switching states u^+/u^- are determined from hitting condition; the trajectory point of the system will approach the local reachability condition (Eq. (4)). The existence conditions can be determined by Lyapunov's second method:[8]

$$\lim_{\sigma \to 0} \sigma \cdot \dot{\sigma} < 0 \quad (5)$$

The time derivation of the sliding line equation for the existence condition becomes

$$\dot{\sigma} = \begin{cases} \lambda_1, & \varsigma > \sigma(x) > 0 \\ \lambda_2, & -\varsigma < \sigma(x) < 0 \end{cases} \quad (6)$$

Where ς is a small quantity. The reconfiguration of switching function and sliding surface from the Eq. (4) is given by:[19]

$$\ddot{\sigma}(x) = \frac{C}{\beta}[k_1 x_1 + k_2 x_2] = Qx \quad (7)$$

Where $Q = [(C/\beta)k_1, (C/\beta)k_2]$; and $x = [x_1 \ x_2]^T$; the conditions for SM control to exist on the modified sliding surface $\ddot{\sigma}(x)$ are

$$\lambda_1 = \left(\frac{C}{\beta}k_1 - \frac{k_2}{\beta R_L}\right)x_2 - \frac{1}{\beta L}k_2 x_1 + \left(\frac{V_{ref} - \beta V_{in}}{\beta L}\right)k_2 < 0 \quad (8)$$

$$\lambda_2 = \left(\frac{C}{\beta}k_1 - \frac{k_2}{\beta R_L}\right)x_2 - \frac{1}{\beta L}k_2 x_1 + \left(\frac{V_{ref}}{\beta L}\right)k_2 > 0 \quad (9)$$

Based on above Eqs. (8), (9), the ranges of k_1 and k_2 can be determined. Where λ_1 and λ_2 are the time derivative of Eq. (7) for two different conditions of Eqs. (8) and (9).

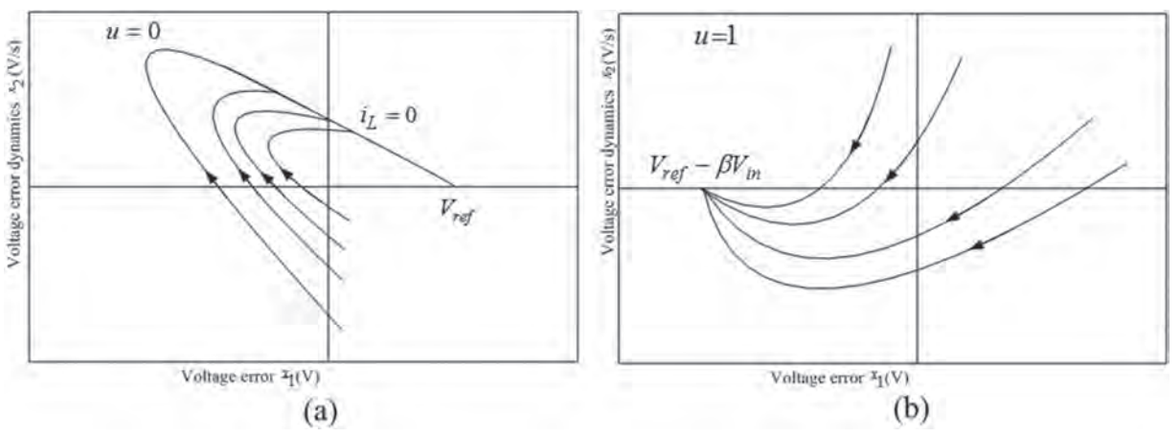


Fig. 2. Phase trajectories of the substructure (a) when $u = 0$ (b) when $u = 1$.

The selected sliding co-efficients should obey Eq. (5), in order to satisfy the existence condition.

3. DESIGN METHODOLOGY OF PROPOSED DIGITAL SM CONTROLLER

The output voltage of the controller satisfying the sliding surface conditions can be represented as[11, 19]

$$\sigma(x) = \frac{1}{\beta R_L}(V_{\text{ref}} - \beta V_0) - i_c \tag{10}$$

From above equation, the coefficients are $k_1 = 1/\beta R_L$ and $k_2 = -1$. Hysteresis modulation based SM controller is basically a type of signum function and realized by a switch relay which is implemented in the FPGA. The output signal is a variable-duration binary, used for generating pulses to the buck converter. This HMSM controller generates variable switching frequency due to hysteresis control, which creates difficulty in design of the circuit components and filter design. Moreover, it is sensitive to disturbances and parametric uncertainties at steady state. To overcome these problems, a fixed frequency controller is presented as follows.

The dynamics of an SM controlled system on an average is similar to a pulse width modulation (PWM) controlled system; therefore the duty-ratio can be configured as a function of discrete pulses in PWM system. This indicates $(u_{\text{eq}} = \ddot{d})$, where $\ddot{d}$ is a duty-ratio which can be defined as:

$$\ddot{d} = \begin{cases} 1, & d \geq 0 \\ d, & 0 < d < 0 \\ 0, & d \leq 0 \end{cases} \tag{11}$$

Hence, it is sensible to design DR-SM based controller where the duty-ratio is regarded as output to generate the gate pulses to the buck converter using a constant frequency component. The SM input can be established with the equivalent control[9] utilizing the invariance conditions $\sigma = 0$ and $\dot{\sigma} = 0$,[8] the equivalent control law can be given by

$$u_{\text{eq}} = \frac{1}{V_{\text{in}}}\left[\left(\frac{LC}{\beta}k_1 - \frac{L}{\beta R_L}k_2\right)x_2 - \frac{k_2}{\beta}x_1 + \frac{V_{\text{ref}}}{\beta}\right] \tag{12}$$

This equation is limited in range of 0 to 1. The value (u_{eq}) and co-efficients can be calculated online as given by Eq. (12). Applying Lyapunov's second method[7, 8]

$$\dot{V}(S) = \sigma \cdot \dot{\sigma} < 0 \tag{13}$$

The Eq. (13) is hold goods when $\sigma = 0$. This can demonstrate the resulted system is stable as well as drives the trajectory to convergence on the sliding-mode surface.

The SM voltage controller is designed in digital platform for DC–DC buck converter with the specifications shown in Table I. The gain coefficient values are calculated in the digital platform (FPGA). The impedance matching circuit is placed between the ADC and buck converter. The sampling frequency is adjusted in ADC by varying the counter parameters. The isolation between the power circuit and control circuit is provided by using opto-coupler MCT2E. The step by step implementation procedure is as follows:

1. The sensed voltage, which is fed to the FPGA, is calculated by designing the resistors R_1 and R_2 as: The setting of the sensed output voltage V_0 is done by voltage divider circuit, which is connected in parallel across the load resistor RL. Suppose if the voltage reference $(V_{\text{ref}}) = 3.3$ V and is fixed by using 3.3 V Zener diode. The attenuation ratio (β) can be calculated by

$$\beta = \frac{V_{\text{ref}}}{V_0} = \frac{3.3}{12} = 0.275 \tag{14}$$

The resistors R_1 and R_2 are related by

$$R_2 = \frac{\beta}{1-\beta} \times R_1 = 0.38R_1 \tag{15}$$

By choosing $R_2 = 330\ \Omega \rightarrow R_1 = 870\ \Omega$.

2. The turns ratios of transformer in the current sensor are 1:100, the sensed capacitor current from the low impedance current sensor (CS1100) is converted into actual value by connecting 100 Ω resistor across the output terminals of the current sensors. The sensed feedback states are sampled in ADC block.

3. The sampled signal from ADC is given to FPGA, to undergo SM control action.

Table I. Buck converter specifications and system parameters.

Parameter	Value
Input voltage range (V_{in})	13–30 V DC
Output voltage (V_{out})	12 V DC
Inductor current ripple (ΔI_L)	30%
Output voltage ripple (ΔV_{out})	500 mV
Switching frequency (f_{sw})	10 kHz
Inductance (L)	110 μH
Capacitance (C)	100 μF
Load resistance (R_L)	10 Ω

Table II. Design equations for buck converter.

Parameter	Design equation	Value
Maximum duty cycle	$D = \frac{V_{\text{out}}}{V_{\text{in}}}$	0.92
Inductor ripple current	$\Delta I_L = (0.3)I_{\text{out(max)}}$	1.2 A
Max switch current	$I_{\text{sw}} = \frac{\Delta I_L}{2} + I_{\text{out(max)}}$	4.6 A
Inductor selection	$L = \frac{V_{\text{out}} \times (V_{\text{in}} - V_{\text{out}})}{f_s \times \Delta I_L \times V_{\text{in}}}$	100 μH
Diode rating	$I_f = I_{\text{out(max)}} \times (1 - D)$	2.4 A
Output capacitor selection	$C_{\text{out}} > \frac{\Delta I_L}{8 \times f_s \times \Delta V_{\text{out}}}$	100 μF
Output capacitor voltage ripple	$\Delta V_{\text{out(ESR)}} = \text{ESR} \times \Delta I_L$	36 mV

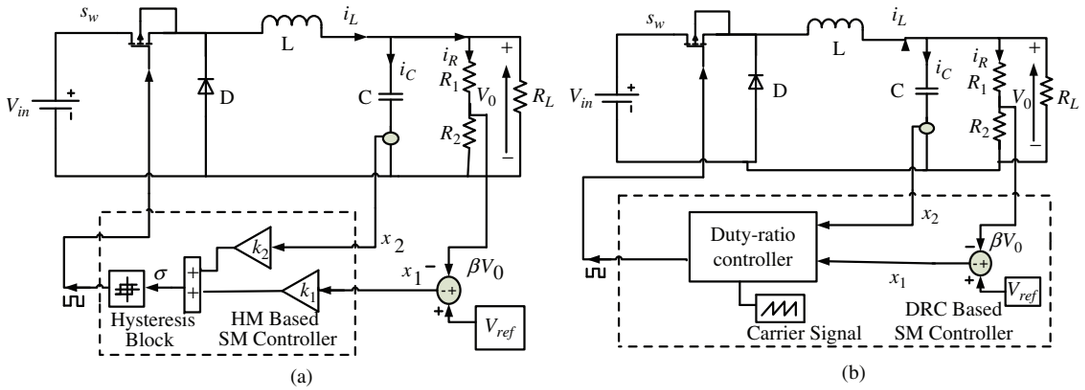


Fig. 3. Block diagram of (a) HM-based SM controller (b) proposed DR-based SM controller.

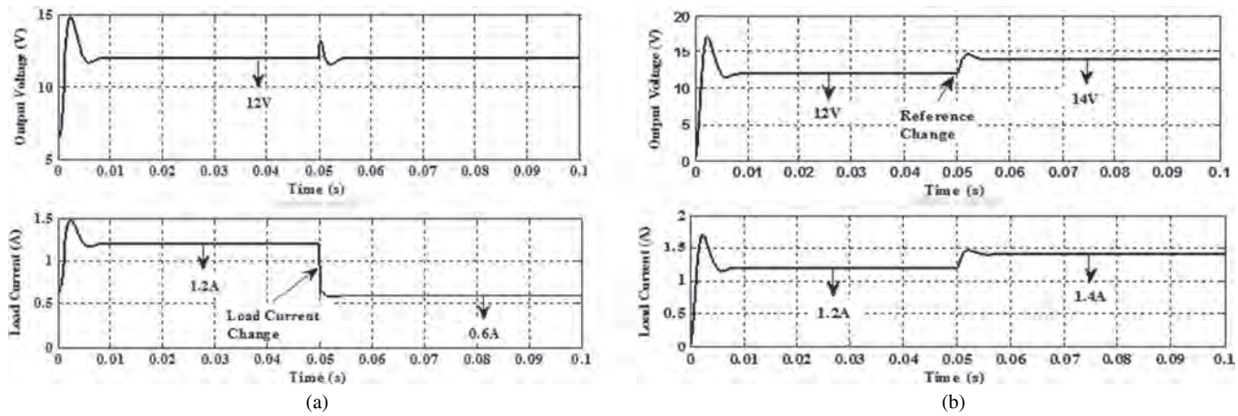


Fig. 4. The output voltage and current of the buck converter using PID controller (a) load current from 1.2 A to 0.6 A at 0.05 seconds (b) voltage reference change from 12 V to 14 V at 0.05 seconds.

4. The reference voltage V_{ref} is generated internally in the FPGA, by setting constant value. The designed sliding coefficients can be easily implemented by setting the gain blocks k_1 and k_2 in the FPGA.
5. For HM-SM controller, the setting of designed hysteresis band is possible with the help of counters in HM block.
6. The control signal (σ) is passed through the HM block, where the gate pulse signal is produced based on the control signal and hysteresis band.
7. For proposed DR-based SM controller, the resultant control law (u) is compared with the internally generated duty-cycle signal for the production of switching pulses.
8. The generated pulse from the control board is given to switch via gate driver IC (MC34151), which amplifies the gate pulse for the proper operation of MOSFET.

4. SIMULATION AND EXPERIMENTAL RESULTS

4.1. Simulation Results

To validate the performance of the closed loop control of SM controllers for DC–DC buck converter, simulation studies have been carried out using MATLAB/Simulink for the specifications shown in Table I. The design specifications for buck-converter and determination of component values based on the design equations[42, 43] are given in Table II. The block diagram of HM-SM and proposed DR-SM controllers are shown in Figures 3(a) and (b) respectively. The robustness of the controller is tested by varying the input voltage, output reference voltage and load of DC–DC buck converter. The output voltage characteristics of the buck converter during load current from 1.2 A to 0.6 A (10 to 20) at 0.05 seconds using PID controller,[29, 44] HM-SM controller[19] and proposed DR-SM controller are shown in Figures 4(a), 5(a) and 6(a) respectively. The reference voltage is changed from the 12 V

Table III. Buck converter performance comparison with different controllers.

Controller type	Initial transients		V_{ref} (12 V → 14 V)		I_L (1.2 A → 0.6 A)	
	PO (%)	t_s (ms)	PO (%)	t_s (ms)	PO (%)	t_s (ms)
PID	23.41	10.2	5.7	5	10	8
HM-SM	0	1.5	0	1	0	0
DR-SM	0	1.6	0	1.1	1.6	0.5

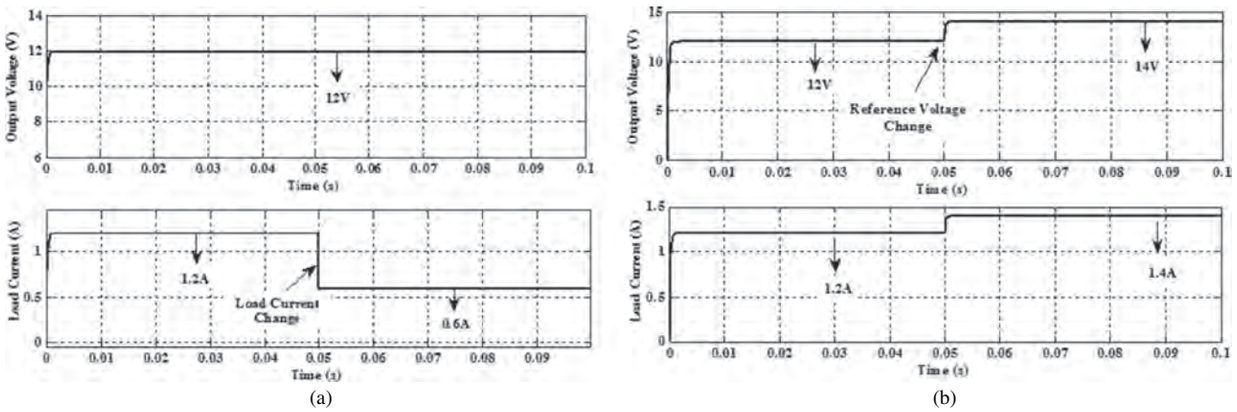


Fig. 5. The output voltage and current of the buck converter using HM-SM controller (a) load current from 1.2 A to 0.6 A at 0.05 seconds (b) voltage reference change from 12 V to 14 V at 0.05 seconds.

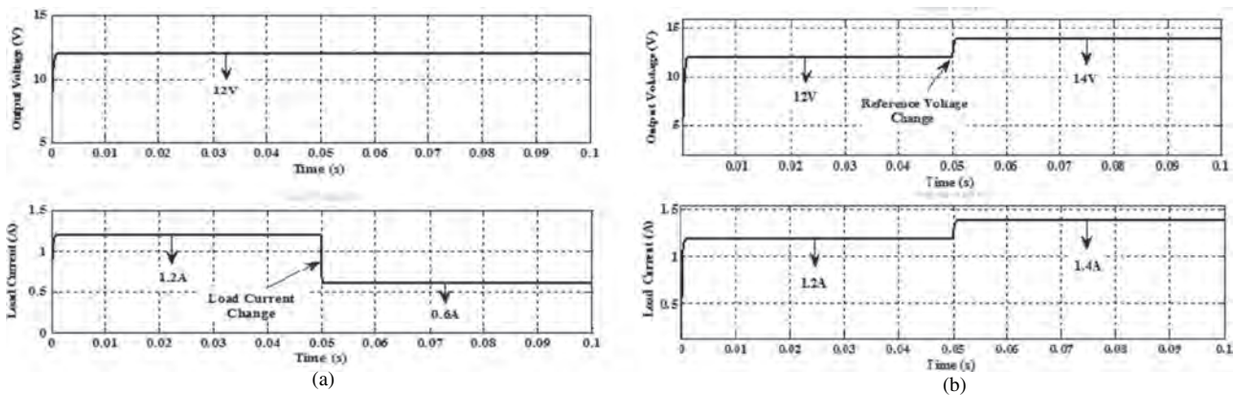


Fig. 6. The output voltage and current of the buck converter using proposed DR-SM controller (a) load current from 1.2 A to 0.6 A at 0.05 seconds (b) voltage reference change from 12 V to 14 V at 0.05 seconds.

to 14 V at 0.05 seconds, the output voltage characteristics of the buck converter using PID controller, HM-SM controller and DR-SM controller is shown in Figures 4(b), 5(b) and 6(b) respectively. The initial overshoots during the change in load and voltage reference are absent in HM-SM and DR-SM controllers. Moreover, smaller settling time in the output voltage of DC–DC buck converter when compared to the PID controller. The performance comparison between different controllers in terms of peak overshoot (PO) and settling time (t_s) are listed in Table III.

4.2. Experimental Setup and Results

To demonstrate the effectiveness of proposed control technique, an experimental prototype of the buck converter is

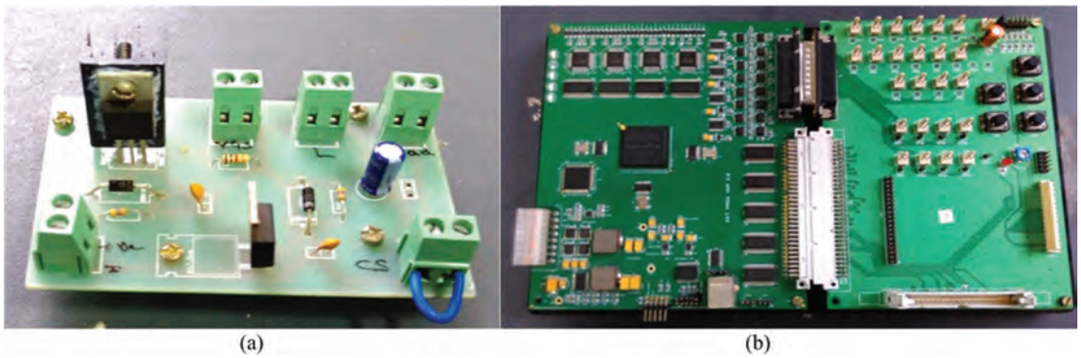


Fig. 7. (a) DC–DC buck converter (b) FPGA board used for SM control.

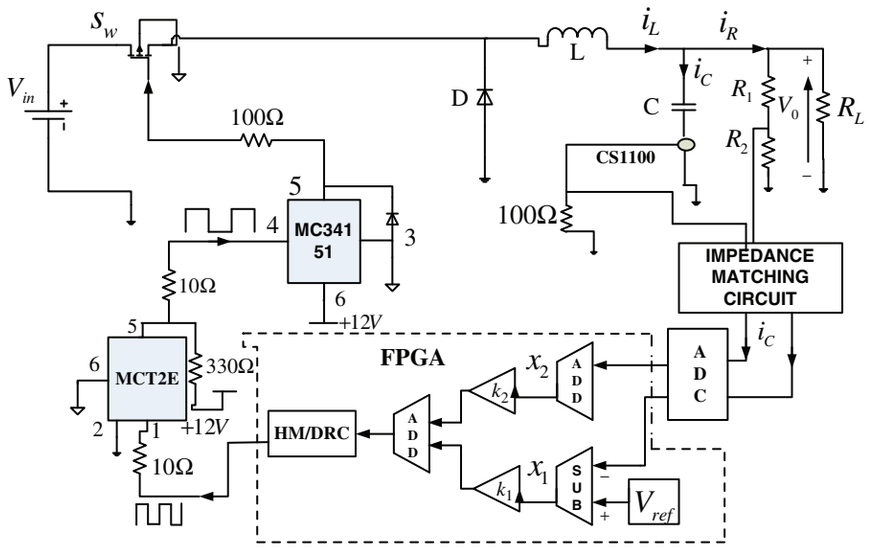


Fig. 8. Buck converter with digital HM/DR-based SM controller.

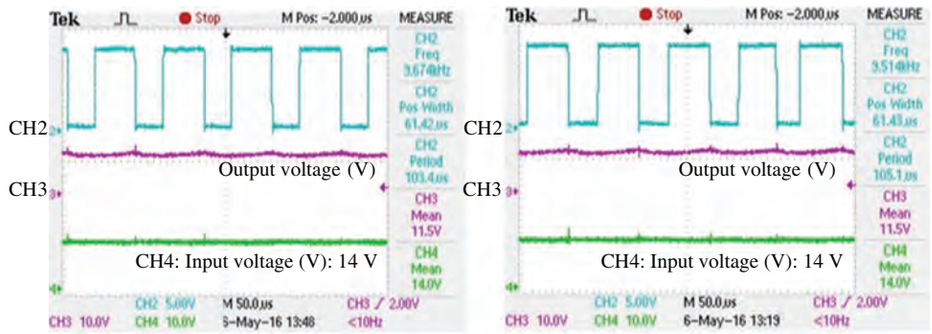


Fig. 9. Gate pulses (CH2: 5 V/div) and output voltage (CH3: 10 V/div) of buck converter with (a) HM based SM controller (b) DR based SM controller with the input voltage of 14 V (CH4: 10 V/div).

developed as shown in Figure 7(a). The SM control law for HM and DR-SM scheme is implemented by using field programmable gate array (FPGA) is shown in Figure 7(b). The block diagram of the digital SM controller using FPGA implementation is shown in Figure 8. The step by step implementation procedure of SM controllers is described in Section 3. The performance of controller is tested by giving different input values to DC–DC buck converter. The converter should maintain constant output voltage for different input voltages. Figures 9–11 shows

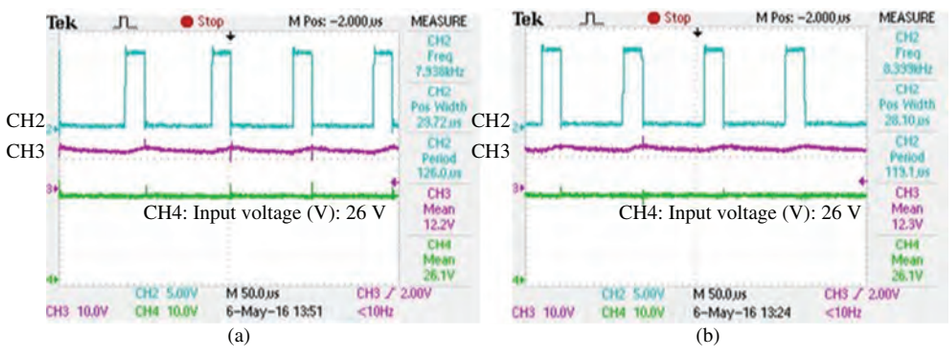
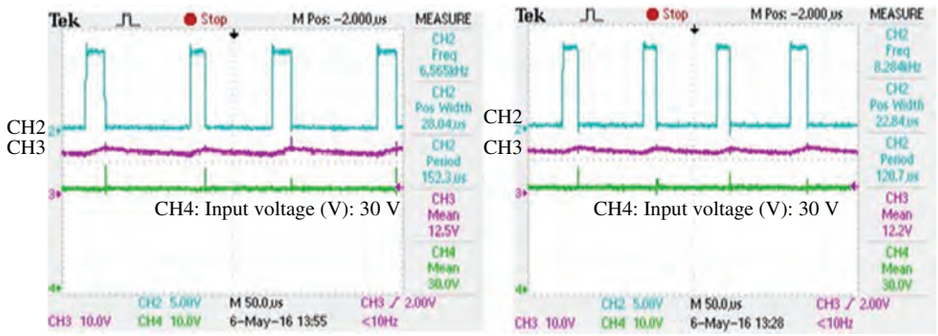
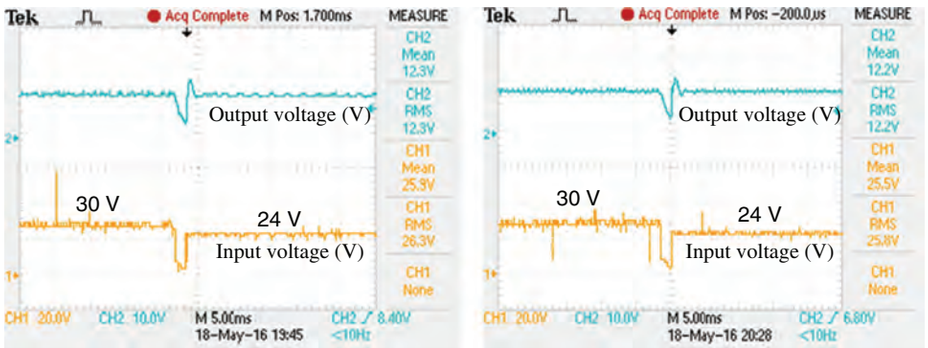


Fig. 10. Gate pulses (CH2: 5 V/div) and output voltage (CH3: 10 V/div) of buck converter with (a) HM based SM controller (b) DR based SM controller with the input voltage of 26 V (CH4: 10 V/div).



(a) (b)

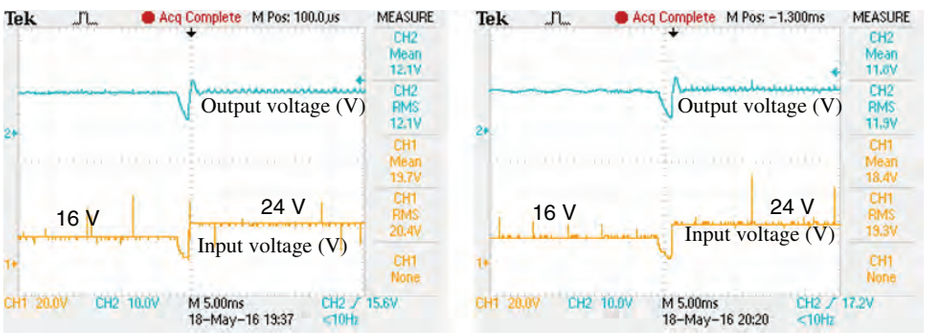
Fig. 11. Gate pulses (CH2: 5 V/div) and output voltage (CH3: 10 V/div) of buck converter with (a) HM based SM controller (b) DR based SM controller with the input voltage of 30 V (CH4: 10 V/div).



(a) (b)

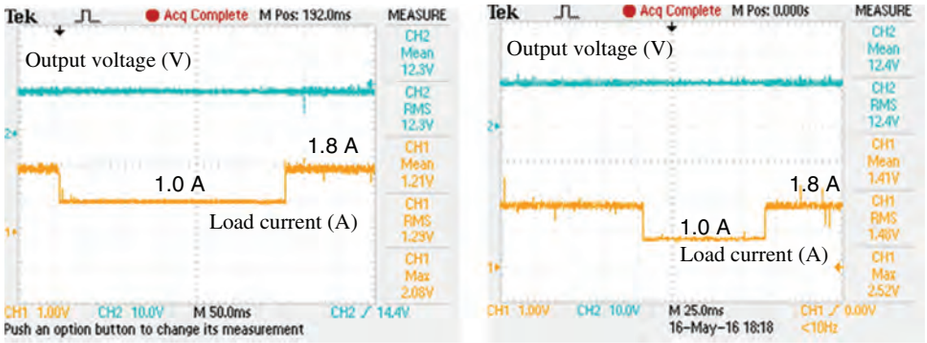
Fig. 12. Output voltage characteristics (CH2: 10 V/div) of buck converter with (a) HM-based SM controller (b) proposed DR-based SM controller with the input voltage variation from 30 V to 24 V (CH1: 20 V/div).

the steady state performance of the buck converter using HM-SM and DR-SM controllers at different voltages 14 V, 26 V and 30 V respectively. The switching frequency is varying from 6.5 kHz to 10.2 kHz using HM-SM controller, (Figs. 9–11(a)) where as it remains constant at 10 kHz (Fig. 9–11(b)) for the variation in input voltage from 14 V to 30 V. The output voltage characteristics of buck converter using HM based SM controller and DR controller for the step change in input voltage from 30 V to 24 V is shown in Figures 12(a) and (b) respectively. The buck converter with PWM based SM controller experiences the peak overshoot of 35% in the output voltage with 3 ms settling time, whereas HM-SM controller peak overshoot of 33% with a settling time of 2 ms during the step change in input voltage from 30 V to 24 V. Similarly, the output voltage response of DC–DC buck converter with HM-SM and DR-SM controllers, for the step change in input voltage from 16 V to 24 V is shown



(a) (b)

Fig. 13. Output voltage characteristics (CH2: 10 V/div) of buck converter with (a) HM based SM controller (b) proposed DR-based SM controller with the input voltage variation from 16 V to 24 V (CH1: 20 V/div).



(a) (b)

Fig. 14. Output voltage characteristics (CH2: 10 V/div) of buck converter with (a) HM-based SM controller (b) proposed DR-based SM controller with the the step change in load current from 1.8 A to 1.0 A (CH1: 1 A/div).

Table IV. Performance comparison of controllers.

Performance index	PID controller	HM-SM controller	Proposed DR-SM controller
Compensator design	Difficult	Easy	Easy
Large signal dynamic performance	Low	High	Medium
Converter model	Small signal	Large signal	Large signal
Special technique requirements	Yes	No	No
Number of sensors	One	Two	Two
Load regulation	Poor	Good	Excellent
Line regulation	Poor	Good	Excellent
Switching frequency	Fixed	Variable	Fixed
Controller implementation	Difficult	Easy	Easy

in Figures 13(a) and (b) respectively. The buck converter experiences the peak overshoot of 33% with a settling time of 2 ms in case of HM-SM controller, whereas DR controller experiences peak overshoot of 32% with settling time of 3 ms during the step change in input voltage from 16 V to 24 V. The robustness of the both controllers (HM and DR) in terms of load regulation (from 1.8 A to 1.0 A) is verified on buck converter as shown in Figures 14(a) and (b) respectively. The output voltage maintained constant without any peak overshoot with both the controllers during step change in load current. The proposed controller performs similar to HM-SM controller; however DR-SM controller overcomes the problem of variable switching frequency as in HM-SM controller. The comparison of DR-SM controller with HM-SM and linear PID controller are listed in Table IV.

5. CONCLUSION

A constant frequency sliding-mode (SM) based duty-ratio digital controller for the voltage regulation of a buck converter is proposed. The various design aspects and comprehensive review on sliding mode controllers are also provided. An experimental prototype and the controller implementation in the FPGA platform are developed to demonstrate the effectiveness of the proposed SM controller. The simulation and experiments results validate the performance of the control scheme and its results are compared with hysteresis modulation based SM control as well as conventional linear controllers. A simple and self-explanatory implementation procedure for the digital controller is also illustrated. Different dynamic tests with line and load changes are performed to check the robustness and functionalities of the system. It is concluded from the results that the proposed duty-ratio based SM voltage controllers successfully solve the problem of variable switching frequency which helps in accurate design of the circuit components and filter design.

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